HITACHI
SERVICE MANUAL

TK | No. 2748E

VT-2700A(U,C)
VT-2805A

Technical Information

VHS
THIS VIDEO DECK IS A VHS TYPE VIDEO RECORDER.
FOR PROPER OPERATION, ONLY THE VHS TYPE CASSETTE MUST BE USED.

Manuals related to the VT-2700A/VT-2805A

Name of Manual	Language	Manual No.		Chapters included
		VT-2700A	VT-2805A	
Technical Data	English	2727E	2635E	Chapters 1-6
Adjustment	French	2728F	—	Chapters 3, 4
Technical Information	English	2748E	2748E	—

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

VIDEO CASSETTE RECORDER

December 1987 **TOKAI WORKS**

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1. COMPARISON TABLES

1-1 COMPARISON WITH PREVIOUS MODEL

	ITEM	VT-2700A	VT-2600A
FEATURES	RECORDING/PLAYBACK FORMAT	S-VHS	VHS
	HQ(HIGH QUALITY)	PROVIDED	PROVIED
	COMB FILTER	PROVIDED (Y, CHROMA)	PROVIDED (CHROMA)
	LEVEL METER SWITCH	PROVIDED	NOT PROVIDED
	VIDEO DUB	PROVIDED	NOT PROVIDED
	AUDIO DUB	PROVIDED	NOT PROVIDED
	MICROPHONE JACK	PROVIDED	NOT PROVIDED
	P in P	PROVIDED	NOT PROVIDED
	P in P SHIFT	PROVIDED	NOT PROVIDED
	TV in TV	PROVIDED	NOT PROVIDED
	MEMORY STOP	PROVIDED	NOT PROVIDED
	STROBE	NOT PROVIDED	PROVIDED
	ART	PROVIDED (SPEED CAN BE VARIED)	PROVIDED (SPEED CAN BE VARIED)
	12-PICTURE MULTI SCREEN	PROVIDED (SPEED CAN BE VARIED)	NOT PROVIDED
	DRPS	PROVIDED (VISS)	NOT PROVIDED
	SCANAPLAY	PROVIDED (VISS)	NOT PROVIDED
	30-SEC SKIP	PROVIDED	PROVIDED
	HIGH-SPEED SEARCH	PROVIDED (2-SPEED)	PROVIDED (2-SPEED)
	PRINTER CONTROL	NOT PROVIDED	PROVIDED (WITH REMOTE CONTROL)
	TIMER RECORDING PROGRAMS	8 PROGRAMS/1 YEAR	8 PROGRAMS/1 YEAR
	TIMER BACKUP TIME	ABOUT 10 MINUTES	ABOUT 5 MINUTES
	PROGRAMMING WITH REMOTE CONTROL	NOT PROVIDED	PROVIDED
	TIME SET WITH REMOTE CONTROL	NOT PROVIDED	PROVIDED
	O.S.D (SUPERIMPOSING)	PROVIDED	PROVIDED
	BLUE BACKGROUND	PROVIDED	PROVIDED
	CALENDAR DISPLAY	PROVIDED (100 YEARS)	PROVIDED (100 YEARS)
	POWER EJECT OFF	PROVIDED	PROVIDED
	DIGITAL TRICK PLAY	PROVIDED	PROVIDED
	CHANNEL TUNING	F.S TUNING (167 CH)	F.S TUNING (120 CH)
CHASSIS	BASIC CHASSIS TYPE	Z	Z
	VIDEO HEADS	3 + Hi-Fi HEADS SP/EP REC/PB: 2 TRICK PB: 1 FM REC/PB: 2	4 + Hi-Fi HEADS SP REC/PB: 2 EP REC/PB: 2 FM REC/PB: 2
		FLYING ERASE: 1	———
	S-VHS DETECTION SWITCH	PROVIDED	NOT PROVIDED
	CAPSTAN DRIVE SYSTEM	DIRECT DRIVE	DIRECT DRIVE
	HALF LOADING	PROVIDED	NOT PROVIDED

1-2 COMPARISON WITH PREVIOUS MODEL

	ITEM	VT-2805A	VT-2605A
FEATURES	RECORDING/PLAYBACK FORMAT	S-VHS	VHS
	HQ(HIGH QUALITY)	PROVIDED	PROVIED
	COMB FILTER	PROVIDED (Y, CHROMA)	PROVIDED (CHROMA)
	LEVEL METER SWITCH	PROVIDED	NOT PROVIDED
	VIDEO DUB	PROVIDED	NOT PROVIDED
	AUDIO DUB	PROVIDED	NOT PROVIDED
	MICROPHONE JACK	PROVIDED	NOT PROVIDED
	P in P	PROVIDED	NOT PROVIDED
	P in P SHIFT	PROVIDED	NOT PROVIDED
	TV in TV	PROVIDED	NOT PROVIDED
	MEMORY STOP	PROVIDED	NOT PROVIDED
	STROBE	NOT PROVIDED	PROVIDED
	ART	PROVIDED (SPEED CAN BE VARIED)	PROVIDED (SPEED CAN BE VARIED)
	12-PICTURE MULTI SCREEN	PROVIDED (SPEED CAN BE VARIED)	NOT PROVIDED
	DRPS	PROVIDED (VISS)	NOT PROVIDED
	SCANAPLAY	PROVIDED (VISS)	NOT PROVIDED
	30-SEC SKIP	PROVIDED	PROVIDED
	HIGH-SPEED SEARCH	PROVIDED (2-SPEED)	PROVIDED (2-SPEED)
	PRINTER CONTROL	NOT PROVIDED	PROVIDED (WITH REMOTE CONTROL)
	TIMER RECORDING PROGRAMS	8 PROGRAMS/1 YEAR	8 PROGRAMS/1 YEAR
	TIMER BACKUP TIME	ABOUT 10 MINUTES	ABOUT 5 MINUTES
	PROGRAMMING WITH REMOTE CONTROL	NOT PROVIDED	PROVIDED
	TIME SET WITH REMOTE CONTROL	NOT PROVIDED	PROVIDED
	O.S.D (SUPERIMPOSING)	PROVIDED	PROVIDED
	BLUE BACKGROUND	PROVIDED	PROVIDED
	CALENDAR DISPLAY	PROVIDED (100 YEARS)	PROVIDED (100 YEARS)
	POWER EJECT OFF	PROVIDED	PROVIDED
	DIGITAL TRICK PLAY	PROVIDED	PROVIDED
	CHANNEL TUNING	F.S TUNING (120 CH)	F.S TUNING (120 CH)
CHASSIS	BASIC CHASSIS TYPE	Z	Z
	VIDEO HEADS	4 + Hi-Fi HEADS SP REC/PB: 2 EP REC/PB: 2 FM REC/PB: 2	4 + Hi-Fi HEADS SP REC/PB: 2 EP REC/PB: 2 FM REC/PB: 2
		FLYING ERASE: 1	———
	S-VHS DETECTION SWITCH	PROVIDED	NOT PROVIDED
	CAPSTAN DRIVE SYSTEM	DIRECT DRIVE	DIRECT DRIVE
	HALF LOADING	PROVIDED	NOT PROVIDED

1-3 COMPARISON OF MAIN CONTROL ICs

ITEM		VT-2700A		VT-2600A	
VIDEO	Y COMB FILTER	HES8023A	(IC1201)	———	
	S-VHS/VHS SWITCH	HT4675D	(IC1202)	———	
	S-VHS SUBEMPHASIS	HT4676D	(IC1203)	———	
	MODE DISCRIMINATOR	HT4677D	(IC1204)	———	
	S-VHS Y PROCESSOR	HT4843B	(IC1205)	———	
	5 MHz PEAKING	HT4685C	(IC1206)	———	
	Y/C MIXER	HT4639A	(IC1251)	———	
	SWITCH	LA7220	(IC1252)	———	
	DIGITAL OUTPUT Y/C SEPARATOR	HES8023A	(IC1253)	———	
	AMP	HT4684A	(IC1254)	———	
	VHS Y PROCESSOR	HT4882	(IC201)	HT4842C	(IC201)
	Y VERTICAL PROCESSOR	HT4853A	(IC202)	HT4843B	(IC202)
	VHS HQ DETAIL ENHANCER	HA11888	(IC203)	HA11888	(IC203)
	CHROMA PROCESSOR	HT4866	(IC204)	HT4866	(IC204)
	CCD 1H DELAY	HT4692	(IC205)	HT4609	(IC205)
	CHROMA COMB FILTER	HES8022AS	(IC206)	HES8022A	(IC206)
	CORRELATIVE NOISE CANCELLER	HES8030	(IC208)	———	
	PLAY EQUALIZER	HES8032F	(IC210)	———	
AUDIO	IN-OUT SELECT/MODE SELECT	HA12117NT	(IC501)	HA12117NT	(IC501)
	FM AUDIO PROCESS	HA12118NT	(IC503)	HA12118NT	(IC503)
	PEAK NOISE REDUCTION	HA12114NT	(IC401)	HA12114NT	(IC401)
	ELECTRONIC VR	M51131L	(IC402)	M51131L	(IC402)
MPX	MPX DECODER	SBX-1436	(IC1301)	SBX-1436	(IC1301)
TUNING	TUNING INTERFACE	μPC1484CA	(IC801)	μPC1484CA	(IC801)
	AFC DET	μPC393	(IC802)	μPC393	(IC802)
OSD	OSD μP	M50455-003	(IC1401)	M50454-004	(IC1401)
	SYNC SEPARATOR	NJM2229S	(IC1402)	LA7808	(IC1403)
	SYNC DETECTOR	NJM2229S	(IC1402)	NJM2220S	(IC304)
SERVO	SPEED/PHASE CONTROL	HD49721N	(IC601)	HD49721N	(IC601)
	TRICK PLAY CONTROL	M54874P	(IC602)	M54874P	(IC602)
	CYLINDER MOTOR DRIVER	HA13455	(IC603)	HA13455	(IC603)
	CAPSTAN SERVO CORRECTOR	HES8018	(IC604)	HES8018	(IC604)
	3.58MHz REF SIGNAL SELECT	BX7519	(IC605)	BX7519	(IC605)
SYSTEM CONTROL	SYSTEM CONTROL μP	ICP14088SB76	(IC901)	HD4074008A03	(IC901)
	LOADING MOTOR DRIVER	BA6209U2	(IC902)	BA6209U2	(IC902)
	VISS CONTROL	HES8026D	(IC904)	———	
TIMER	TIMER μP	ICP75216-046	(IC751)	M50955-306	(IC751)
	HEADPHONE AMP	M5218L	(IC752)	M5218L	(IC752)
REGULATOR	MULTI-REGULATOR	STK5372	(IC851)	STK5372	(IC851)
	5V REGULATOR	L780S05	(IC871)	L780S05	(IC871)
	-6V REGULATOR	AN79N06	(IC861)	AN79N06	(IC861)
	5V REGULATOR	NJM78M05	(IC881)	———	
DIGITAL PROCESS	AGC	M51489L	(IC1001)	———	
	SYNC SEPARATOR, MAIN/SUB SCREEN SWITCH	NJM2227	(IC1002)	NJM2217L	(IC1016)
	DIGITAL μP	μPD7508HG	(IC1003)	μPD7508HG	(IC1010)
	Y/C MIXER	HA11525	(IC1004)	———	
	P in P CHROMA DECODER	HA11532	(IC1005)	———	
	CHROMA D/A CONVERTER	HA19507	(IC1006)	HA19507MP	(IC1006)
	VIDEO A/D CONVERTER	HA19216M	(IC1007)	HA19216M	(IC1007)
	CHROMA D/A CONVERTER	HA19507	(IC1008)	———	
	MPX	MSA137MS-K	(IC1009)	MSA137MS-K	(IC1009)
	30 nS DELAY	HT4666A	(IC1011)	HT4666A	(IC1011)
	COUNTER	BA225F	(IC1012)	BA235AF	(IC1012)
	MULTI H CORRECTOR	TC74HC123FP	(IC1013)	———	
	OSC	HT4682	(IC1014)	———	
	TRICK PLAY CONTROLLER	HG40B38F	(IC1015)	HG62H40B38F	(IC1001)
	MULTI CONTROLLER	HG62B40B41F	(IC1016)	———	
	P in P CONTROLLER	HG61H25B51F	(IC1017)	———	
	FIELD MEMORY	M5M4C264	(IC1018-IC1022)	HM5046P	(IC1002-IC1005)
	SYNC SEPARATOR	BX6350	(IC1024)	HT4667	(IC1008)
PRE/REC AMP	PRE/REC AMP (V)	HA118021MP	(IC2)	HA118021MP	(IC1)
	PRE/REC AMP (A)	HA12115MP	(IC1)	HA12115MP	(IC2)

COMPARISON OF MAIN CONTROL ICs

ITEM		VT-2805A		VT-2605A	
VIDEO	Y COMB FILTER	HES8023A	(IC1201)	———	
	S-VHS/VHS SWITCH	HT4675D	(IC1202)	———	
	S-VHS SUBEMPHASIS	HT4676D	(IC1203)	———	
	MODE DISCRIMINATOR	HT4677D	(IC1204)	———	
	S-VHS Y PROCESSOR	HT4843B	(IC1205)	———	
	5 MHz PEAKING	HT4685C	(IC1206)	———	
	Y/C MIXER	HT4639A	(IC1251)	———	
	SWITCH	LA7220	(IC1252)	———	
	DIGITAL OUTPUT Y/C SEPARATOR	HES8023A	(IC1253)	———	
	AMP	HT4684A	(IC1254)	———	
	VHS Y PROCESSOR	HT4862	(IC201)	HT4842C	(IC201)
	Y VERTICAL PROCESSOR	HT4853A	(IC202)	HT4843B	(IC202)
	VHS HQ DETAIL ENHANCER	HA11888	(IC203)	HA11888	(IC203)
	CHROMA PROCESSOR	HT4866	(IC204)	HT4866	(IC204)
	CCD 1H DELAY	HT4692	(IC205)	HT4609	(IC205)
	CHROMA COMB FILTER	HES8022AS	(IC206)	HES8022A	(IC206)
	CORRELATIVE NOISE CANCELLER	HES8030	(IC208)	———	
	PLAY EQUALIZER	HES8032F	(IC210)	———	
AUDIO	IN-OUT SELECT/MODE SELECT	HA12117NT	(IC501)	HA12117NT	(IC501)
	FM AUDIO PROCESS	HA12118NT	(IC503)	HA12118NT	(IC503)
	PEAK NOISE REDUCTION	HA12114NT	(IC401)	HA12114NT	(IC401)
	ELECTRONIC VR	M51131L	(IC402)	M51131L	(IC402)
MPX	MPX DECODER	SBX-1436	(IC1301)	SBX-1436	(IC1301)
TUNING	TUNING INTERFACE	μPC1484CA	(IC801)	μPC1484CA	(IC801)
	AFC DET	μPC393	(IC802)	μPC393	(IC802)
OSD	OSD μP	M50455-003	(IC1401)	M50454-004	(IC1401)
	SYNC SEPARATOR	NJM2229S	(IC1402)	LA7808	(IC1403)
	SYNC DETECTOR	NJM2229S	(IC1402)	NJM2220S	(IC304)
SERVO	SPEED/PHASE CONTROL	HD49721N	(IC601)	HD49721N	(IC601)
	TRICK PLAY CONTROL	M54874P	(IC602)	M54874P	(IC602)
	CYLINDER MOTOR DRIVER	HA13455	(IC603)	HA13455	(IC603)
	CAPSTAN SERVO CORRECTOR	HES8018	(IC604)	HES8018	(IC604)
	3.58MHz REF SIGNAL SELECT	BX7519	(IC605)	BX7519	(IC605)
SYSTEM CONTROL	SYSTEM CONTROL μP	HD4074008A03	(IC901)	HD4074008A03	(IC901)
	LOADING MOTOR DRIVER	BA6209U2	(IC902)	BA6209U2	(IC902)
	VISS CONTROL	HES8026D	(IC904)	———	
TIMER	TIMER μP	M50955-306	(IC751)	M50955-306	(IC751)
	HEADPHONE AMP	M5218L	(IC752)	M5218L	(IC752)
REGULATOR	MULTI-REGULATOR	STK5373	(IC851)	STK5372	(IC851)
	5V REGULATOR	———		L780S05	(IC871)
	-6V REGULATOR	AN79N06	(IC861)	———	
DIGITAL PROCESS	AGC	M51489L	(IC1001)	———	
	SYNC SEPARATOR, MAIN/SUB SCREEN SWITCH	NJM2227	(IC1002)	NJM2217L	(IC1016)
	DIGITAL μP	μPD7508HG	(IC1003)	μPD7508HG	(IC1010)
	Y/C MIXER	HA11525	(IC1004)	———	
	P in P CHROMA DECODER	HA11532	(IC1005)	———	
	CHROMA D/A CONVERTER	HA19507	(IC1006)	HA19507MP	(IC1006)
	VIDEO A/D CONVERTER	HA19216M	(IC1007)	HA19216M	(IC1007)
	CHROMA D/A CONVERTER	HA19507	(IC1008)	———	
	MPX	MSA137MS-K	(IC1009)	MSA137MS-K	(IC1009)
	30 nS DELAY	HT4666A	(IC1011)	HT4666A	(IC1011)
	COUNTER	BA225F	(IC1012)	BA235AF	(IC1012)
	MULTI H CORRECTOR	TC74HC123FP	(IC1013)	———	
	OSC	HT4682	(IC1014)	———	
	TRICK PLAY CONTROLLER	HG40B38F	(IC1015)	HG62H40B38F	(IC1001)
	MULTI CONTROLLER	HG62B40B41F	(IC1016)	———	
	P in P CONTROLLER	HG61H25B51F	(IC1017)	———	
	FIELD MEMORY	M5M4C264	(IC1018-IC1021)	HM5046P	(IC1002-IC1005)
	FIELD MEMORY	MB81461	(IC1022)	———	
	SYNC SEPARATOR	BX6350	(IC1024)	HT4667	(IC1008)
PRE/REC AMP	PRE/REC AMP (V)	HA118021MP	(IC2)	HA118021MP	(IC1)
	PRE/REC AMP (A)	HA12115MP	(IC1)	HA12115MP	(IC2)

2. PROGRAM INDEX

2-1. GENERAL DESCRIPTION

PROGRAM INDEX is the system that records the INDEX signals made by modulating the CTL pulse width during (1) STOP -RECORD (including Timer REC and IRT), (2) STOP PAUSE - REC PAUSE -RECORD, (3) PLAY PAUSE - REC PAUSE - RECORD and (4) RECORD -REC PAUSE - RECORD (in recording Audio only mode) and that detects this INDEX signals during Scanner operation then plays it back for approx. 10 seconds.

When the INDEX button on the front panel or remote hand unit is pressed in the STOP mode, the VTR will wait whether the operator inputs a two-digit index number or operates SCAN AND PLAY.

Pressing the FF or REW button will cause VTR to start SCAN AND PLAY.

When the 10-key numeric pad, two digits of desired program number, and SEEK button on the remote hand unit are pressed, the VTR will start searching the desired index number and will play it back approximately 10 seconds.
Then the index mode is cancelled and playback mode continues.

2-2. RECORDING THE INDEX SIGNAL (Fig. 2-1)

The Program Index System records the CTL (control) pulses coded as "0" and "1" on the CTL pulse track, as index signals that locate the starts of programs during play, for a certain period (about 2 seconds) immediately after a recording is started. The CTL pulse is configured as follows so that it does not affect the servo operation during normal play. The "0" pulse is a normal CTL pulse.

"0" pulse: duty 60% (recording cycle: 33.3 msec)
"1" pulse: duty 30% (recording cycle: 33.3 msec)

The index signal consists of 61 "1" pulses that are recorded continuously and it is discriminated when (32 - 58) continuous "1" pulses are detected.

Note: The widths of the index signal detected vary at different tape speeds.

The index signal is recorded automatically at the timing shown in Table 2-1.

Table 2-1 Index Record Modes and Timing

Operation mode	Index record timing
Timer recording, IRT STOP - RECORD	Immediately before recording starts
STOP PAUSE - REC PAUSE - REC STILL - REC PAUSE - REC	Immeadiately before recording starts
REC PAUSE - REC only audio recording from external input (without sync)	Immediately before recording starts

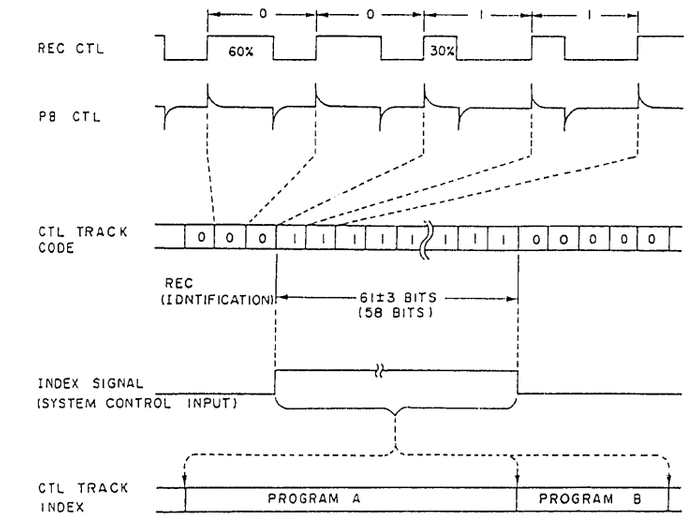


Fig. 2-1 Developing the Index Signal

2-3. SCANNER PLAY

When scanner operation (F.F, REW ON) is performed with INDEX ON, the VTR enters the play mode for 10 seconds when the index signal is detected (See Fig. 2-2).

Fig. 2-3 shows 2 types of scanner play sequences depending on during F. FWD/REW mode.

When the F. F, REW, PLAY or STOP is operated during scanner play period (10 sec), the VTR enters the operated mode.

The index signals should be recorded with an interval of 5 minutes or more. This interval is provided so that the VTR will not enter the scanner operation by detecting the same index signal when REW is to be operated during the scanner period in the REW mode.

2-4. INDEX CIRCUIT OPERATION

2-4-1. CTL pulse shaping (Fig. 2-4(A))

Normally, the duty of the CTL pulse is 60% (Called "0" pulse). To apply the information to the CTL pulse in a model

with the INDEX function, its duty is varied to 60% (the "0" pulse) and 30% (the "1" pulse) and recorded on the CTL track.

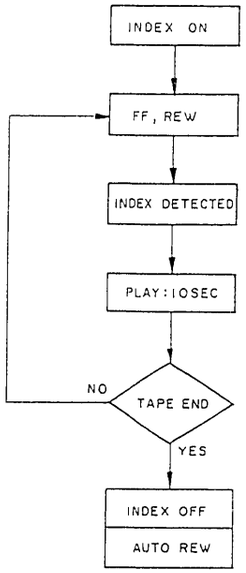


Fig. 2-2 Scanner Operation

The phase of the CTL signals must be controlled correctly so that the capstan servo works normally during both forward play and reverse play and also when "1" pulses are reproduced. IC904 is a module consisting of the INDEX µP and its peripheral circuits which shape the CTL pulse and control its phase. The following describes the operation of the peripheral circuits.

The CTL pulse applied to pin 4 is shaped by IC601 (Servo IC). The OP AMP-2 shapes the CTL pulse to a square wave. The comparison reference input to the inverting terminal of OP AMP-2 can be switched by Sl to approx. 1/2 Vcc.

- When a positive pulse is input, OP AMP-2 outputs "Hi" to set Sl forcibly to "Hi". Therefore. if the pulse input stops, OP AMP-2 continues to output "Hi".
- When a negative pulse is input, OP AMP-2 outputs "Lo" and will maintain "Lo" in the reverse way to the above after the pulse input stops.

As shown above, OP AMP-2 maintains "Hi" when a positive pulse is switched to negative and "Lo" in the opposite way. As a result, the CTL pulse is shaped into a square wave. The CTL pulse shaped by this circuit has the relationship shown in Fig. 2-5 "CTL pulse input/output timing chart".

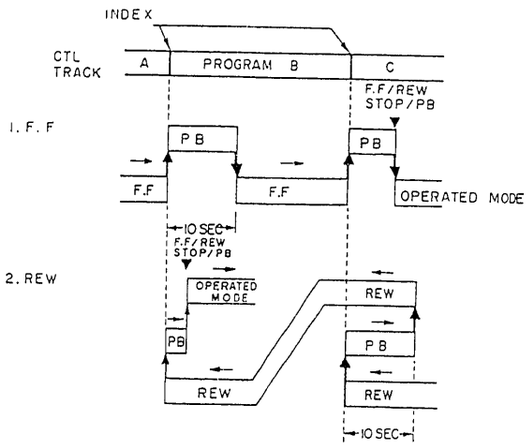
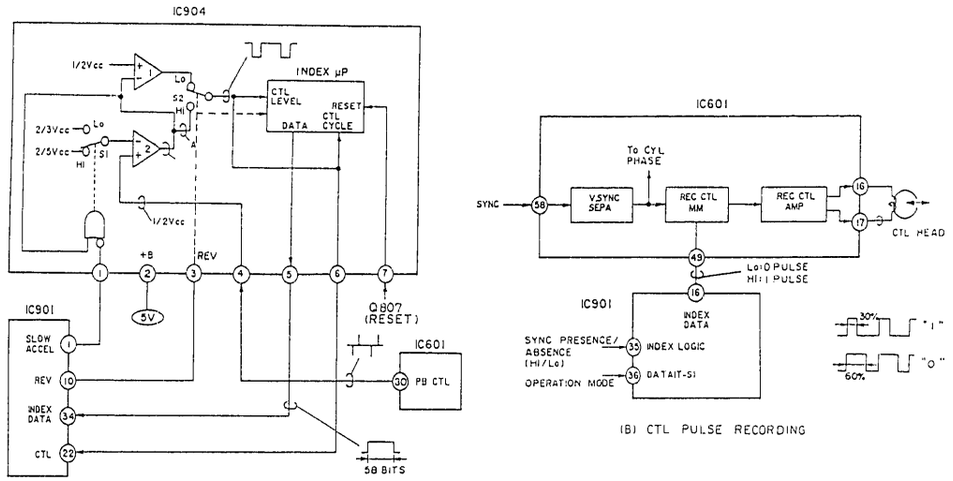


Fig. 2-3 Scanner Sequence



(A) CTL PULSE PLAYBACK

(B) CTL PULSE RECORDING

Fig. 2-4 Index Circuit

If the servo circuit does not control the positions of the CTL pulses correctly, the tape feed and tracing of the heads do not match. This can also apply to the reverse operation. The servo is operated by the pulse indicated by the arrow in forward play. Since this pulse is used to maintain the same relationship in reverse play, the polarities of the pulses detected are completely reverse in controlling the servo operation. OP AMP-1 corrects the relation of these polarities. To discriminate "0" or "1" from the duty of the CTL pulses, the period from the fall of one pulse to that of the next pulse is used. Therefore, OP AMP-1 inverts the CTL pulse only in forward play and supplies it to the INDEX µP. This provides the relation of CTL pulse phases betwen forward play and reverse play shown in the Fig. 2-6. The INDEX µP uses these pulses to discriminate "0" or "1".

2-4-2. CTL pulse "0", "1" recording and discrimination (Fig. 2-4(B))

(See the timing chart of the INDEX µP input CTL pulse and recording current in Fig. 2-7.)

The CTL pulse "0" and "1" are defined as Table 2-2 depending on its duty at the input of INDEX µP (pin 6 of the module).

Table 2-2 "0", "1" Definition

	"0" pulse	"1" pulse
Recording	60%	30%
Forward play	40%	70%
Reverse play	60%	30%

The duty of CTL pulse is switched by the DC level at pin 49 of IC601.

Lo: "0" pulse with 60% duty
Hi: "1" pulse with 30% duty

Then, the CTL pulse is supplied to the CTL head through IC601 pins 16 and 17. IC901 (system control µP) outputs a signal via pin 16 to control IC601. It controls the output at pin 16 as Table 2-3 depending on the operation mode.

Table 2-3 IC901 CONTROL

PIN 35	PIN 36	PIN 16	INDEX
Hi	Recording	Hi while INDEX signal is written at the start of recording	Possible
Hi	Recording pause to recording	Remains Lo at the start of recording	Impossible
Lo	Recording	Hi while INDEX signal is written at the start of recording	Possible
Lo	Recording pause to recording	Hi while INDEX signal is written at the start of recording	Possible

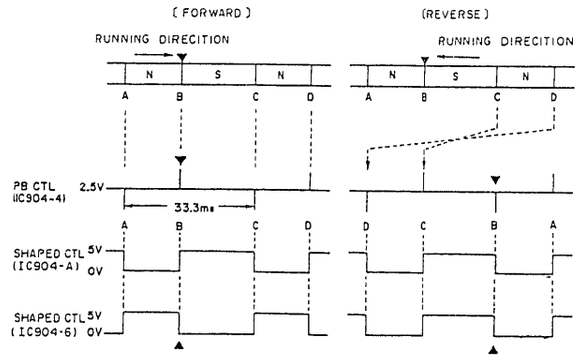


Fig. 2-5 CTL Pulse Input/Output Timing Chart

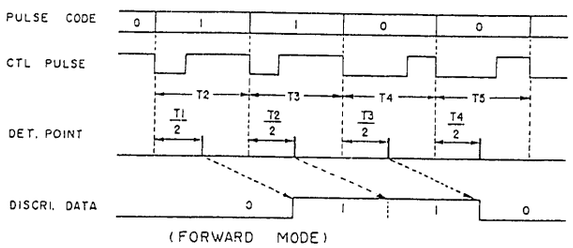


Fig. 2-6 "0", "1" Data Discrimination

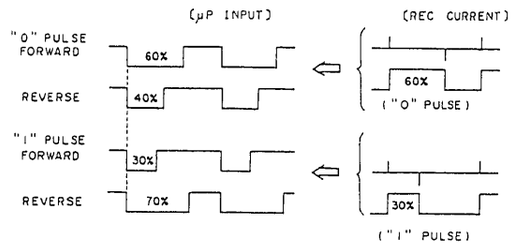


Fig. 2-7 CTL Pulse and Rec Current

Meantime, the playback CTL pulse "0" or "1" is discriminated as follows. The INDEX μP always monitors the cycle of the CTL pulse and measures the level of the CTL half cycle after its fall (strictly speaking, a 1/2 cycle of one pulse before). This level is as in Table 2-4 in forward and reverse play.

Table 2-4 CTL Pulse Level

	"0" pulse	"1" pulse
Forward play	Lo	Hi
Reverse play	Hi	Lo

Since the levels in the half cycle are reverse between reverse play and forward play, the INDEX μP uses the REVERSE signal from the system control μP to invert the discrimination data and then outputs the data. Therefore, the correction output at pin 5 is as in Table 2-5.

Table 2-5 Correction Output

	"0" pulse	"1" pulse
Forward play	Lo	Hi
Reverse play	Lo	Hi

3. MULTI-PICTURE FUNCTION

3-1. General Description

Following the P in P and trick play/digital video effects that have started to apply the IC memories which have rapidly become less expensive to VTRs, this new model provides a multi-picture system that allows a multi slow motion (called the "multi-strobe" hereafter) effect for continuous photographic playback and a multi-channel facility which can display the TV programs of all active channels by switching the tuner in sequence.

3-1-1. Basic configuration (Figs. 3-1, 3-2)

Figs. 3-1 and 3-2 show the basic configuration of the digital video block in this model and the memory configuration.

The input/output switch IC1002, A/D converter IC1007 and D/A converter IC1006 and IC1008 are used in common for trick play, multi-picture and P in P modes. Though omitted from Fig. 3-1, each controller which controls these three modes receives commands from the system control μP and timer μP through the digital μP.

Concerning the memory configuration, a dual-port D-RAM is used for the P in P memory (two D-RAMs are used in the previous model VT-1570A). The memory for trick play consists of 7 exclusive field memories (6 for 6-bit and one for read sync) in the previous model, but in this new model, the DPCM (Differential Pulse Code Modulation) system is used as will be described in "TRICK PLAY" to reduce the required memory capacity greatly and 4 dual-port D-RAMs are used. For the multi-picture function, all these 5 memories for P in P and trick play are used. Therefore, the P in P memory IC1022 is connected to P in P controller IC1017 and multi-picture controller IC1016 and the trick play memories IC1018 - IC1021 are connected to trick play controller IC1015 and multi-picture controller IC1016 for control.

3-1-2. Basic functions

The basic functions of the multi-picture system are shown in Table 3-1.

Table 3-1 Multi-picture functions

Multi-picture Function	System Control Status
MULTI EE STROBE	STOP, FF, REW
MULTI CHANNEL	STOP, FF, REW
MULTI PB STROBE	PB
MULTI SLOW STROBE	SLOW
MULTI STILL STROBE	STILL
MULTI INDEX (AUTO)	STOP, FF, REW
MULTI INDEX (MANUAL)	STOP, FF, REW

(1) The EE/PB/SLOW/STILL STROBE functions are so-called "photographic playback" functions and allow 12 pictures (3 vertical x 4 horizontal) to be displayed in sequence at the selected speed in still playback, and only the last picture displayed is moving. The display speed can be selected in 6 steps, infinity, 2, 1, 1/2, 1/5, 1/30 seconds, by operating the slow speed up/down buttons. In the infinity interval mode, the small moving picture will be shifted manually by using "F.ADV" button. However, in the SLOW mode, the slow speed is used, and in the STILL mode, one picture is stored in memory every time the F.ADV pulse is received to shift the moving picture.

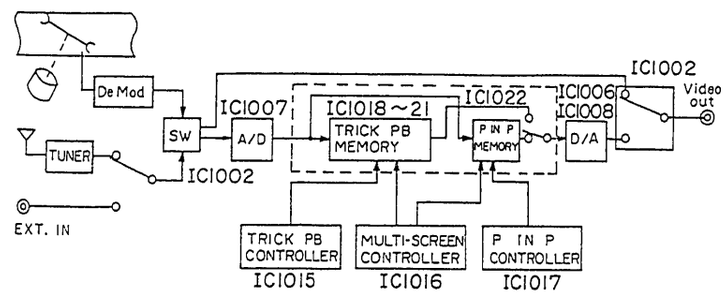


Fig. 3-1 Basic Configuration of Digital Video Block

(2) The MULTI-CHANNEL function is so-called "channel index". It stores up to 12 channels from the bottom number in the channel list in memory every time the CH UP pulse is received in the TV reception mode, and the last channel provides a moving picture. After displaying 12 pictures has been completed, all the pictures become still.

(3) The MULTI-INDEX (AUTO) function is so-called "tape index". When this mode is entered, the tape is rewound to its start and is then played back. When an index signal recorded on the tape is detected, the picture is stored in memory. Then, the next index signal is detected in the fast forward mode and the picture is stored. These operations are repeated automatically until the tape reaches the end or displaying 12 pictures is completed.

(4) The MULTI INDEX (MANUAL) function is also so-called "tape index". Every time the FREEZE button is pressed within 10 seconds of scanner playback after the INDEX signal is detected, the played back picture at the point is stored in memory in sequence. This stored data can be reproduced by operating the RECALL button. However, as long as the stored data is not erased, trick play modes such as still, slow, etc. do not provide a digital picture but an analog picture.

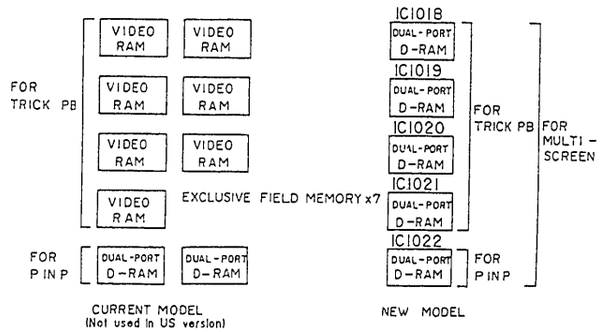


Fig. 3-2 Memory Configuration

3-2. Screen Configuration (Figs. 3-3, 3-4. Tables 3-2, 3-3)

Table 3-2 and Fig. 3-3 show the 1/3-reduction multi-picture display system and frame processing. Since the input signals are sampled from both the first and second fields and written to independent memories, the output signals are interlace-scanned as shown in the figure on the right in Fig. 3-3. Therefore, a moving picture is a frame picture. However, a still picture is a field picture of only the first field because of the memory configuration as described in the next item 3. Concerning the screen display area, the 1/3 reduction ratio would provide a 9-picture multi-system, but one vertical column is added to display 12 pictures, so approx. 70% of a full picture is displayed in the horizontal direction. Since approx. 95% is displayed in the vertical direction, the small picture in the 1/3-reduction 12-picture system becomes approximately a square. However, as the information in a video picture is most at the center and less at the edges, these square pictures are sufficient for multi-pictures used as indexing.

Table 3-2 1/3 Reduction Multi-Screen Display System

Reduction Ratio	NUMBER OF PICTURES	MOVING PICTURE	STILL PICTURE	MEMORY CAPACITY	VERT. DISPLAY AREA	HORIZ. DISPLAY AREA
1/3	12	FRAME	FIELD	1.01Mbit	95%	70%

Table 3-3 Multi-picture specifications

Picture reduction ratio	1/3
Number of displayed pictures	12 (3 vertical x 4 horizontal)
Number of quantized bits	6 bits
Picture size	75H vertical, 12.0 µsec horizontal
Processing signal	Component signal
Write clock frequency	Y: 2/3 fsc, B-Y, R-Y: 1/6 fsc } fsc
Read clock frequency	Y: 2 fsc, B-Y, R-Y: 1/2 fsc } 3 fsc
Display system	Interlaced display

Table 3-3 shows the multi-picture specifications and Fig. 3-4 shows the picture configuration. The number of quantized bits is 6 that is the same for P in P and trick play and a component signal separated into the luminance and color-difference signals from the video signal is used in the same way as in P in P for signal processing because it is difficult to maintain the continuity of chroma signal when the picture is reduced.

As can be seen in Fig. 3-4, one small screen has a display area that is 95% vertical and 70% horizontal of an effective TV picture (without sync and burst signals). The thickness of the edges is 2H vertical and 0.28µsec horizontal.

3-3. Memory configuration (Figs. 3-5, 3-6)

The memory used in this model incorporates 4 sheets of the memory field each of which consists of 256 x 256 bits. Fig. 3-5 shows the memory configuration for one field. One memory field is divided into 3 rows x 5 columns and areas 1 -12 which correspond to those of the picture configuration. Areas A, B and C in the column on the farthest right are the memories for the second field when the picture is moving. As has previously been seen in Table 3-2, a still picture is a field picture but a moving picture is a frame picture in this system, and when a moving picture is provided in areas 1 - 4, 5 - 8 and 9 - 12, areas A, B and C are used respectively as their second field to provide interlaced-scanning.

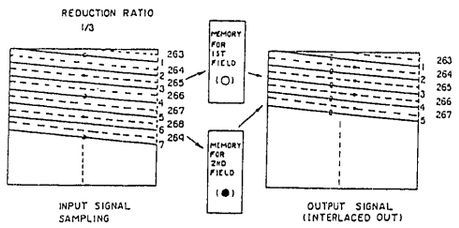


Fig. 3-3 Frame-Accordance Processing

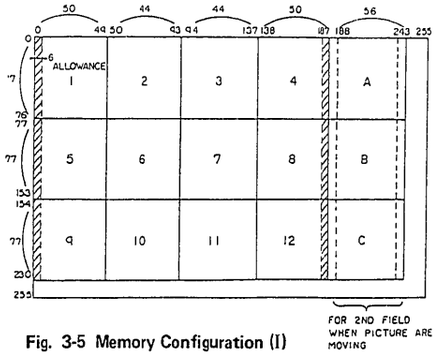


Fig. 3-5 Memory Configuration (I)

The shaded 6 bits on the farthest left in Fig. 3-5 provides an allowance to prevent missing pictures due to drift in the picture display position caused by the TV. 70% of the horizontal memory length shown in Fig. 3-4 corresponds to 44 bits in Fig. 3-5. This allowance is also required on the right of the screen and is provided by 6 bits on the right side of the row of 4, 8 and 12. The row of second field A provides 12 bits of allowance, 6 bits on the left when combined with 1, 5, 9 and 6 bits on the right when combined with 4, 8, 12.

Fig. 3-6 shows the overall configuration of the 5 memory ICs. Since one memory IC has 4 sheets of the memory field consisting of 256 x 256 bits, there are a total of 20 sheets of the memory field. As shown in Table 3-3, the ratio of the sampling frequencies between the luminance and chroma signals is Y : (B-Y)+(R-Y) = 2 : 1. Therefore, as 2Y and 1C are each 6 bits, a total of 18 bits are configured as shown in Fig. 3-6 and only 2 memory fields are used from P in P memory IC1022.

The memory capacity required is 244 x 231 bits x 18 sheets = 1,014,552 bits as can be seen from Figs. 3-5 and 3-6, and approx. 1.01 Mbits as shown in Table 3-2.

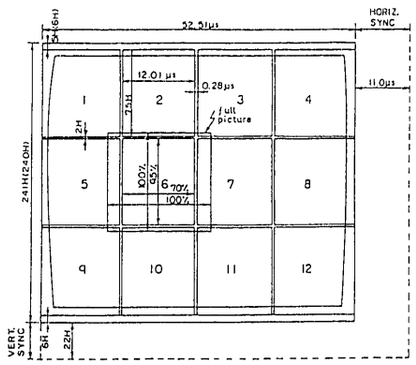


Fig. 3-4 Screen Composition

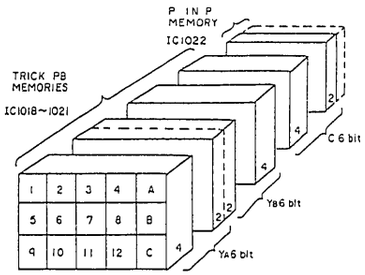


Fig. 3-6 Memory Configuration (II)

3-4. Circuit Configuration (Fig. 3-7)

Fig. 3-7 is a block diagram of the multi-picture system.

3-4-1. P in P switch (IC1002)

The EE video signal supplied from the tuner or LINE IN jack or the PB video signal from the luminance/chroma circuit is selected by input switches S5 and S6 in IC1002 and is added to the signal for a sub picture applied to the chroma decoder IC (IC1005).

3-4-2. Chroma decoder (IC1005)

The video signal selected by P in P switch IC1002 for a sub picture is processed by chroma decoder IC1005 in the same way as in the P in P operation and is separated into the color-difference signals (R-Y, B-Y) and luminance signal (Y).

3-4-3. Multiplexer (IC1009)

The Y signal and the R-Y and B-Y signals output from the chroma decoder are sampled by the line sequential system that is almost the same as in the P in P system and the sampling frequencies (see Table 3-3), and the DC clamp levels matching these three signals are added to these signals as a preparation for A/D conversion in the next stage.

3-4-4. A/D converter (IC1007)

The three signals, Y, B-Y and R-Y, are sampled by the multiplexer in the previous stage to be converted to a time-sharing serial signal and are then converted to a 64-step, 6-bit digital signal to be stored in memory.

3-4-5. Multi-controller (IC1016)

The multi-controller consisting of gate arrays controls the overall multi-picture system.

(1) Input processor
The input processor separates the digital video signal input as a serial signal into Y, R-Y and B-Y and applies these to memory as three signals, YA, YB and C (R-Y/B-Y) as shown in Fig. 3-6 according to the addresses designated by the memory controller.

(2) Memory controller
This is the center of the multi-controller which generates the memory control signals such as timing control signals, address signals for writing/reading, etc.

(3) Y output processor
This not only rearranges the parallel signals, YA and YB, read from the memories to a serial signal (YA/YB) and also adds sync signals because the digital video signals read from the memory do not have sync signals.

(4) C output processor
This not only converts the serial signals (B-Y/R-Y) read from the memory to parallel signals, B-Y and R-Y, and also adds a burst signal because the signals read from memory do not have a burst signal.

(5) Chroma encoder
This synthesizes the NTSC chroma signal from R-Y and B-Y with a burst signal.

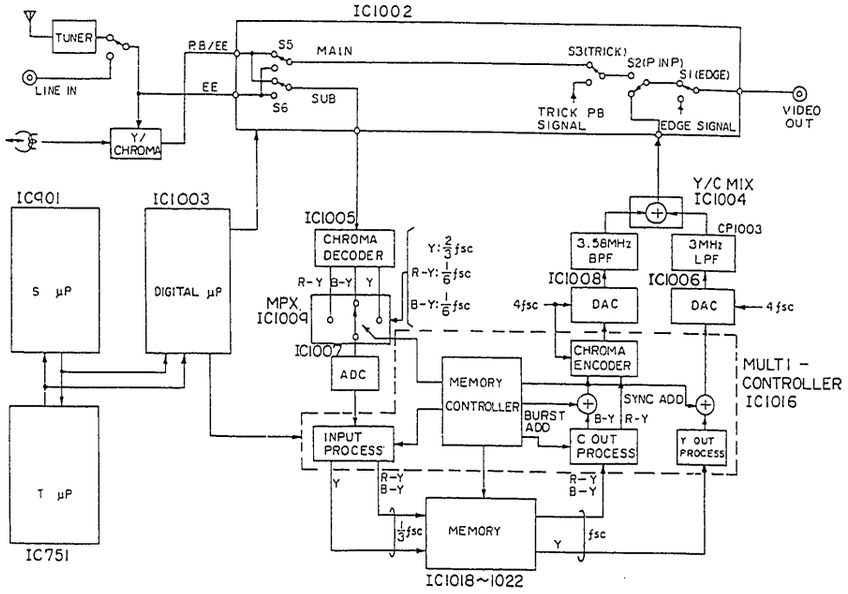


Fig. 3-7 Multi-Screen System Block Diagram

(6) Other sections
The edge signal generator generates the signal to switch EDGE SW S4 in P in P switch IC1002. The gray back controller generates a signal which makes the screens with no pictures gray, the same color as the edges, and applies it to the edge generator.

3-4-6. D/A converter (IC1006, IC1008)

This converts the Y and C digital signals to analog signals. Because of 1/3 reduction, the clock frequencies are three times those in A/D conversion, but 4 fsc is used for the C signal due to the chroma encoder. The high-frequency and clock frequency components generated in D/A conversion are removed by the 3MHz LPF and 3.58MHz LPF respectively.

3-4-7. Y/C mixer (IC1004)

The D/A converted luminance and chroma signals are mixed to form a composite video signal. This operation is the same as in the P in P system.

3-4-8. Output switch (IC1002)

In the multi-picture mode, the composite video signal for multi pictures is always selected by internal switch S2 (P in P). S1 (EDGE) selects the edge signal generator output not only in the edge sections but also in no signal sections to provide the gray background in the no signal areas in 12 picture areas. The output of S4 is connected to the VIDEO OUT jack and RF converter.

3-4-9. Digital μP (IC1003)

The operator's commands and VTR state are transmitted to the digital μP through the timer μP and system control μP respectively to control the overall multi-picture system.

3-5. Circuit Operation

3-5-1. Digital μP and peripheral circuits (Fig. 3-8)

The operation keys (MULTI-PIX, FREEZE, STROBO and RECALL) used in the multi-picture mode are on the front panel and remote controller and their inputs are transferred to the digital μP via the timer μP (T-μP). The reception bus lines are used in common with the communication bus lines between the system control μP (S-μP) and T-μP, which are three lines, DATA (S-D) from the S-μP and DATA (T-D) from the T-μP and clock line CLOCK (S-D) from the S-μP.

There are four output pins used in the multi-picture mode, DIGITAL REC (pin 31), MULTI RECALL (pin 34), WR. PULSE (pin 35) and MULTI (pin 43).

DIGITAL REC (31) is connected to the control pin (3) of video signal select switch IC305. This switch selects the EE or digital video signal and applies it to the recording circuit in the luminance/chroma system. It recalls up to 12 pictures selected by the RECALL key on the TV screen mode and allows them to be recorded in the specified positions on the tape (for example, at the start). MULTI RECALL (34) is an output which goes "Lo" in the MULTI, MULTI RECALL and P in P modes and is applied to the P in P inhibit input, pin 12, of P in P switch IC1002 through OR circuit D1003. This P in P inhibit input is active "Lo" and allows the sub pictures and edges to be inserted. The MULTI RECALL output drives switch Q1017 to disable the MULTI (43) output. This is because the MULTI (43) output continues to be "Hi" after the MULTI mode is released waiting the MULTI RECALL mode, and the MULTI RECALL controls whether the multi pictures are displayed or not.

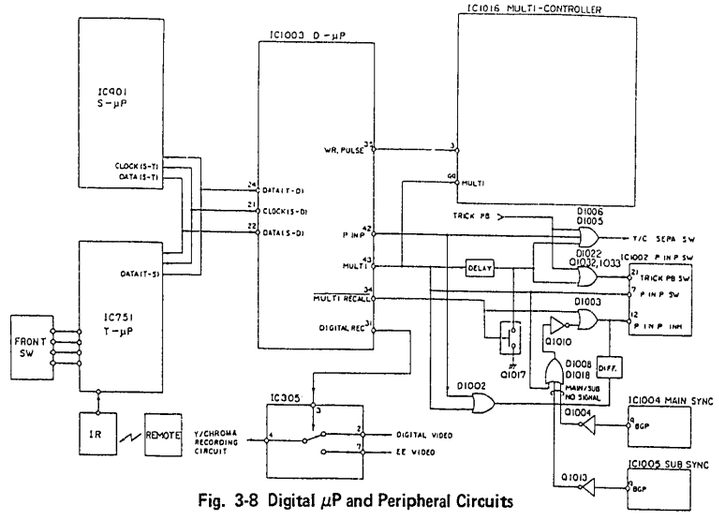
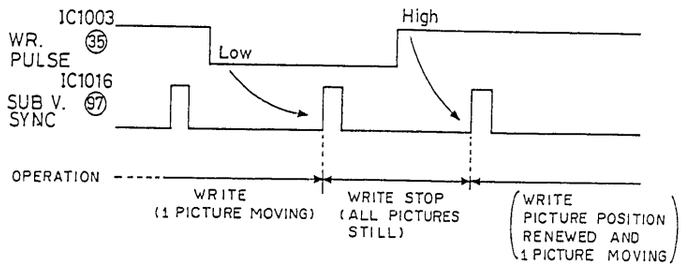


Fig. 3-8 Digital μP and Peripheral Circuits

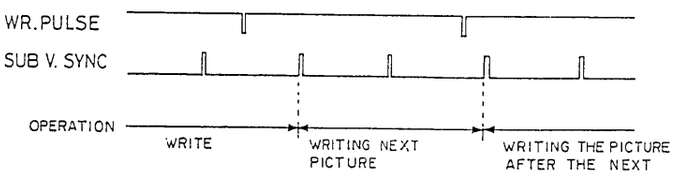
MULTI (43) is a multi-picture mode setting output and controls the P IN P video SW pin 7 of P in P switch IC1002 as well as the multi-controller (IC1016) to always fix this switch to the sub video input side. This output is also applied to the P in P inhibit input of P in P switch IC1002 through OR circuit D1002 and the differential circuit. This differential circuit inhibits appearance of a multi picture for approx. 0.2 seconds to prevent a noisy sub picture from appearing on the TV screen when the multi-picture mode is entered. Then, MULTI (43) passes through the delay circuit and is applied to the trick play SW control input, pin 21 of P in P switch IC1002 and Y/C separation switch in the video circuit through OR circuits D1022 and D1006 respectively. The trick play switch in IC1002 is set to the trick play side in the trick play and multi-picture modes. However, a trick play picture would appear on the TV immediately after the multi-picture mode is entered, affected by the above-mentioned differential circuit. To prevent this, the switch is provided with a delay of approx. 0.3 seconds.

WR. PULSE (35) controls the writing of the multi-picture signal to the memory. As can be seen from the timing chart in Fig. 3-9, it goes "Hi" when a small picture is moving and renews the picture position due to the first input of the write vertical sync signal to start writing, and it goes "Lo" when all pictures are still and stops writing due to the first input of the write vertical sync signal.

(A) BASIC OPERATION



(B) MULTI-STROBE: PICTURE POSITION RENEWED WITH 1 PICTURE MOVING



(C) MULTI-CHANNEL: STILL PICTURE DISPLAYED WHILE SWITCHING CHANNEL

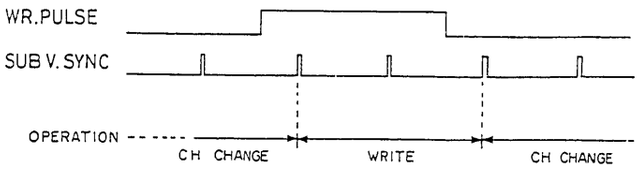


Fig. 3-9 Write Pulse Timing Chart

3-5-2. NTSC demodulator, MPX, A/D converter (Fig. 3-10)

Fig. 3-10 shows the process circuit in which the sub video signal selected by the main/sub video input switch is converted to a digital signal up to its input to the multi-controller.

This circuit consists of the following.

- NTSC demodulator (IC1005) which demodulates the video signal into luminance and color-difference signals.
- Multiplexer (IC1009) which clamps the luminance and color-difference signals within the sampling range of the A/D converter and converts them to serial signals.
- A/D converter (IC1007) which converts the luminance and color-difference signals, converted to serial signals, to a digital signal quantized to 6 bits.
- Multi-controller (IC1016) which controls these three ICs.

(A) IC1005 receives the sub video signal (SUB VIDEO) at pins 5 and 24 and performs the following operations.

1. Generates the burst gate pulse (BGP) necessary to demodulate the color-difference signals.
2. Separates the luminance signal and then limits the bandwidth to less than half the sampling frequency (CP1001: 1.3 MHz LPF).
3. Limits the bandwidth of the R-Y and B-Y color-difference signals to less than half the sampling frequency before demodulating them (CP1004: 3.58 MHz BPF).

(Burst gate pulse (BGP) generation)

To determine the phase of the BGP signal, IC1005 uses the H. SYNC SEPA. to separate the horizontal sync signal from the sub video signal input to pin 5 and applies it to the BGP generator. The BGP generator delays the horizontal sync signal by approx. 2.5 µsec and then shapes it to a square wave with a width of approx. 3.5 µsec. (See Fig. 3-11 (A)). The luminance signal is separated by the 1.3MHz lowpass filter (CP1001) and is limited to less than half the sampling frequency and is then applied to pin 13 of the multiplexer (IC1009).

The color-difference signals, B-Y and R-Y, are demodulated by the same process as in a TV receiver. These color-difference signals are previously limited by the external 3.58MHz BPF to less than half the sampling frequency before being demodulated and are then applied to pins 9 and 11 of IC1009.

IC1005 stops the inputs to the demodulator circuit (R-Y DEMOD, B-Y DEMOD) to reduce noise at the clamp points of the color-difference signals in the horizontal retrace period. This is controlled by the multi-controller output connected to pin 17. The multi-controller generates the control signal (BLP) of the gate using the sync signal separated from the video signal which is selected for a sub picture and outputs it

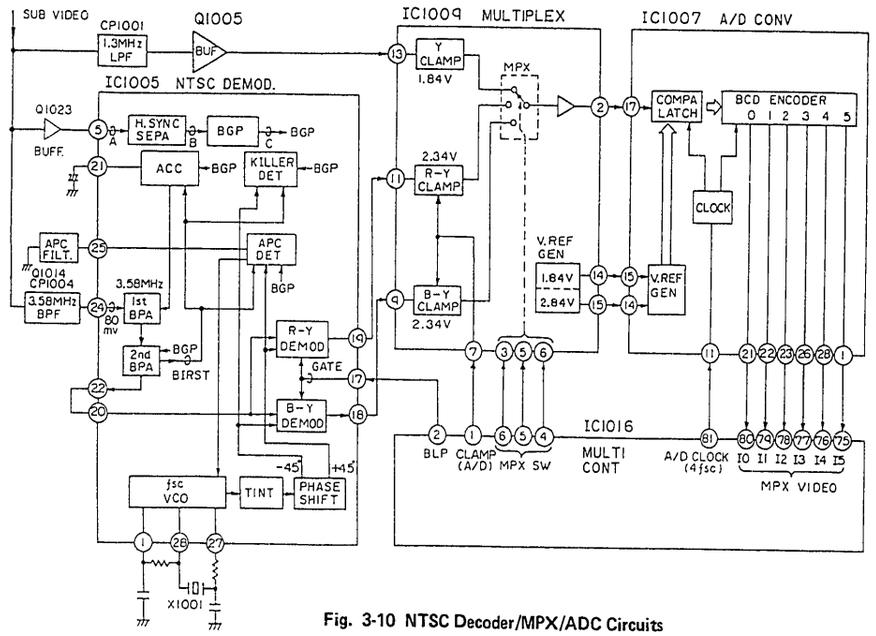


Fig. 3-10 NTSC Decoder/MPX/ADC Circuits

at pin 2. The BLP signal is in phase with the horizontal sync signal and its pulse width is determined to 12 µs, equivalent to the horizontal retrace period. The BLP signal turns off the gates in the R-Y DEMOD and B-Y DEMOD. Therefore, the outputs of the demodulators (R-Y DEMOD, B-Y DEMOD) in IC1005 become signals with reduced noise on the pedestal line. (Fig. 3-11(C))

(B) IC1009 inputs the luminance (Y) and color-difference signals (R-Y, B-Y) from CP1001 and IC1005 via pins 13, 11 and 9 respectively and operates the following.

1. Clamps the sync tip of the luminance signal to 1.84V using the Y CLAMP and clamps the center of the amplitudes of the color-difference signals using the R-Y/B-Y CLAMPs.
2. Converts each signal to a serial signal using the multiplexer (MPX).

The setting voltages of the Y, R-Y and B-Y CLAMPs are obtained by dividing 5V by three ladder resistors in the V REF GEN. The sync tip of the luminance signal (Y) is clamped to 1.84V by Y CLAMP. The center levels of the R-Y and B-Y signals are clamped by R-Y and B-Y CLAMPs to 2.34V, that is 0.5V higher than the luminance sync tip level. Since the maximum amplitude of the Y signal is set to 1V as shown in Fig. 3-11 (B), half the voltage (2.34V) of the maximum amplitude of the Y signal becomes the clamp voltage of the R-Y and B-Y signals. The clamp timing of the R-Y and B-Y signals is determined by the multi-controller. The multi-controller generates a clamp control signal (CLAMP (A/D)) using the horizontal sync signal separated from the video signal which was selected for the sub picture and outputs it at pin 1. The CLAMP (A/D) signal is determined as a pulse with a width of 3.36 µs which is delayed from the trailing edge of the horizontal sync signal by 2.52 µs. (See Fig. 3-11 (C)) This signal is supplied to the B-Y and R-Y CLAMPs via pin 7 of IC1009.

The multiplexer (MPX) receives the clamped Y, R-Y and B-Y signals and converts them to serial signals using the 3-phase MPX control signals supplied from the multi-controller. The multi-controller generates the MPX SW signals (Y MPX SW, B-Y MPX SW, R-Y MPX SW), synchronized with the horizontal and vertical sync signals separated from the video signal which was selected for a sub picture, and outputs them at pins 6, 5 and 4. Sampling of a sub picture is performed at 2/3 fsc for the Y signal and at 1/3 fsc for the color-difference signals (at 1/6 fsc for each R-Y and B-Y) and the sampling order is determined as follows.

The color-difference signals are sampled in the (3n + 1) H periods and the Y signal is sampled in the (3n + 2) H periods.

1st H: (B-Y) - (R-Y) - (B-Y) ---- (R-Y)
2nd H: Y - Y - Y ---- Y
3rd H: not sampled
4th H: (B-Y) - (R-Y) - (B-Y) ---- (R-Y)
5th H: Y - Y - Y ---- Y

The above sampling is called the line sequential system as shown in Fig. 3-12, which is the same as in P in P in principle. In the line sequential system, the color-differene signals (R-Y

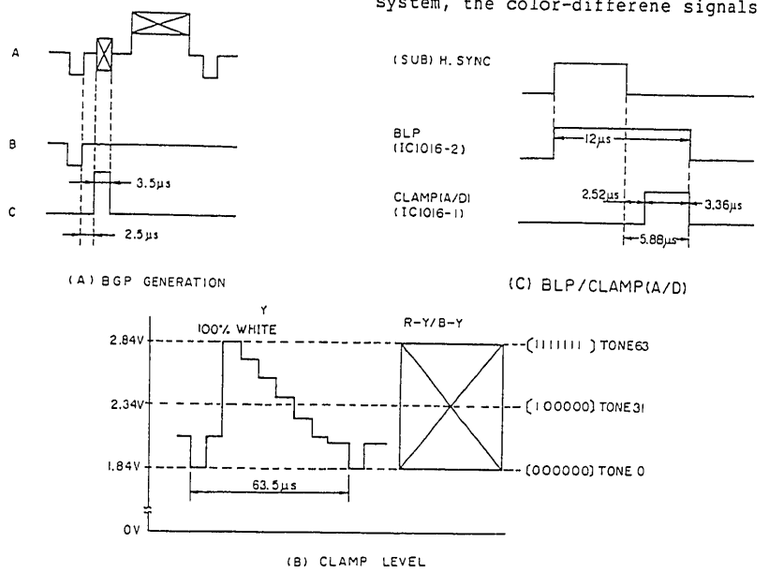


Fig. 3-11 Timing Cahart

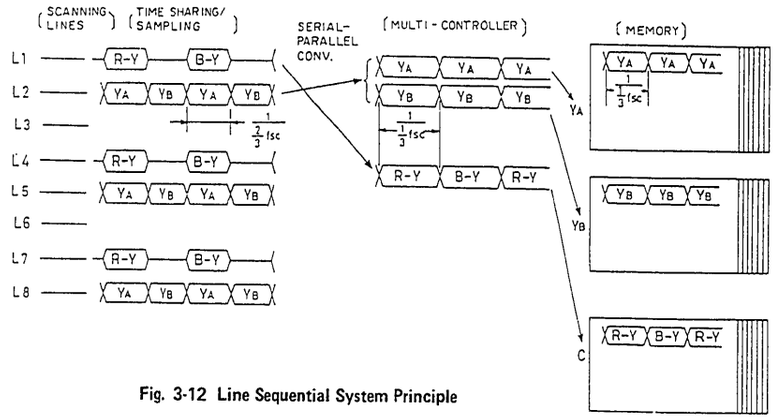


Fig. 3-12 Line Sequential System Principle

and B-Y) are sampled from the L1, L4, L7 --- scanning lines and the Y signal is sampled from the L2, L5, L8 ... scanning lines.

In the line sequential system, the Y/C displacement of 1/3 line component occurs in the vertical direction of a reduced picture in principle, but there is no problem in each sub picture.

Fig. 3-13 shows the MPX operation timing.

The Y, R-Y and B-Y signals converted to serial signals are supplied to pin 2 of IC1009.

IC1007 receives the Y, R-Y and B-Y signals converted to serial signals at pin 17 and converts them to digital signals quantized to 6 bits and then applies them to pins 75 to 80 of the multi-controller.

The reference voltage necessary for A/D conversion is obtained from the reference voltage generator (V REF GEN) at pins 14 and 15 of IC1009 and the clock signal is from pin 81 of the multi-controller. The V REF GEN generates the maximum and minimum reference voltages for A/D conversion. The minimum voltage is determined as 1.84V and the maximum as 2.84V to cope with the maximum input amplitude, 1Vp-p. These two reference voltages are applied to the reference voltage generator (V REF GEN) at pins 15 and 14 of IC1007. This V. REF GEN divides the voltage (1V) obtained by subtracting the minimum voltage (1.84V) from the maximum voltage (2.84V) evenly to 1/64 by the ladder resistors and applies the divided voltages to the comparator/latch circuit (COMPA/LATCH).

The COMPA/LATCH compares the MPX output voltage at pin 17 and the 64-step reference voltage applied from the V REF GEN when the clock signal equivalent to 4 fsc which is supplied from pin 81 of the multi-controller is "Hi", and when the clock signal is "Lo", the COMPA/LATCH is set to a mode in which it latches the comparison result and applies the output to the BCD encoder.

The BCD encoder codes the comparison result of the COMPA/LATCH to 6 bits and applies the outputs to pins 75 to 80 of the multi-controller.

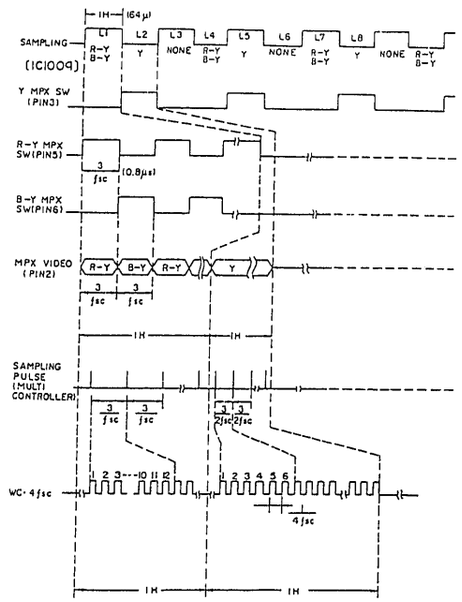


Fig. 3-13 MPX Sampling Timing Chart

3-5-3. Multi-controller circuit (Fig. 3-14)

Fig. 3-14 shows multi-controller IC1016 and its peripheral circuits. Its overview is similar to the P in P controller, but the multi-controller does not have the 6-bit - 4-bit encoder/decoder and there are differences due to the different memory configuration.

(1) Timing controller/memory controller (Figs. 3-15, 16, 17, 18)

The timing controller and memory controller in multi-controller IC1016 are responsible for controlling the operation timing of the overall multi-picture system and the memories and accept the following input signals.

(a) WC. 4 fsc (pin 100), RC. 4 fsc (pin 30)
These are clock signals for writing and reading and are obtained by inverting the 4 fsc output of C-D/A converter IC1008 by the inverter in IC1011. This 4 fsc signal is divided by 4 by the timing control circuit and is output from pin 16. This enters IC1008 via pin 24 and is phase-compared with the color subcarrier in the sub video signal input from pin 3 to control the internal VCO and is phase-matched with 4 fsc.

(b) SUB H. SYNC (pin 98), SUB V. SYNC (pin 97)
These are horizontal and vertical sync signals in the sub video signal and output from IC1005.

(c) MULTI (pin 99), WR. PULSE (pin 3)
These are output from the digital μP. MULTI is the MULTI mode input which sets the mutli-controller to the MULTI mode and makes the output ports of the multi-controller active.

WR. PULSE is a writing-to-memory control pulse input as can be seen from Fig. 3-9. This goes "Hi" when a small picture is moving and renews the picture position due to the first input writing vertical sync signal to start writing, and goes "Lo" when all pictures are still and stops writing due to the first input of the writing vertical sync signal.

The following are the outputs of the timing control circuit.

(d) A/D CLOCK (pin 81), C. D/A CLOCK (pin 32), Y. D/A CLOCK (pin 28)
These are clock signal outputs for A/D, chroma D/A and luminance D/A conversions respectively. The frequencies are -the A/D CLOCK is 2/3 fsc and both C. D/A and Y. D/A CLOCKs are 4 fsc. A/D CLOCK is produced by dividing WC·4 fsc by 6. RC·4 fsc is used without being divided for C. and Y. D/A CLOCKs.

(e) MPX SW Y (pin 6), MPX SW R-Y (pin 5), MPX SW B-Y (pin 4), CLAMP (A/D) (pin 1)

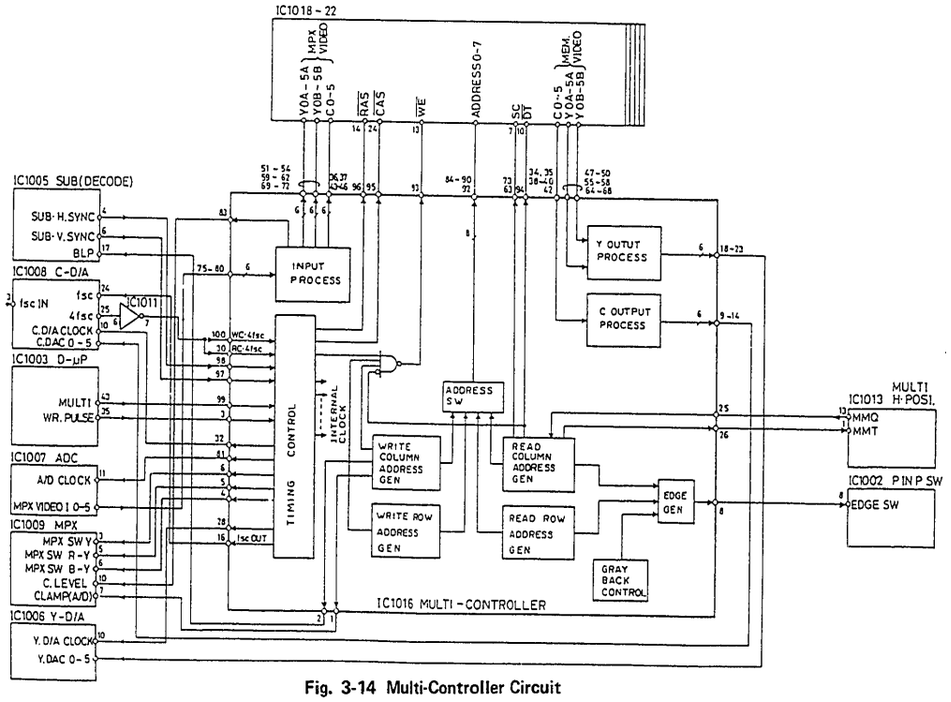


Fig. 3-14 Multi-Controller Circuit

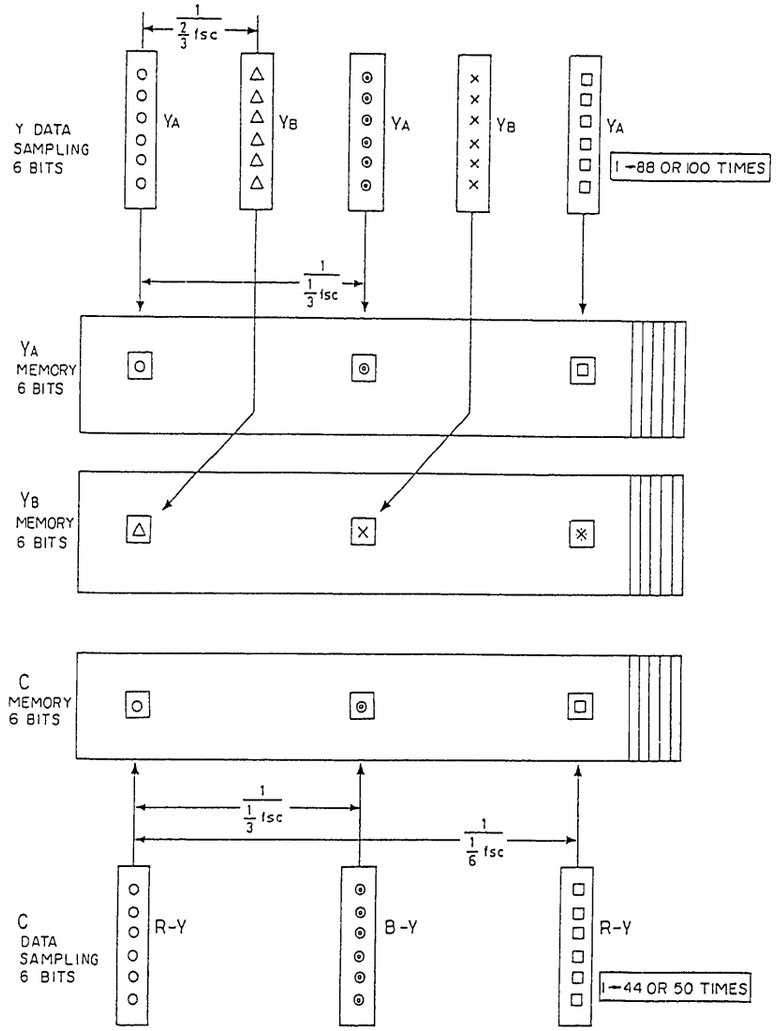


Fig. 3-15 Writing to Memory

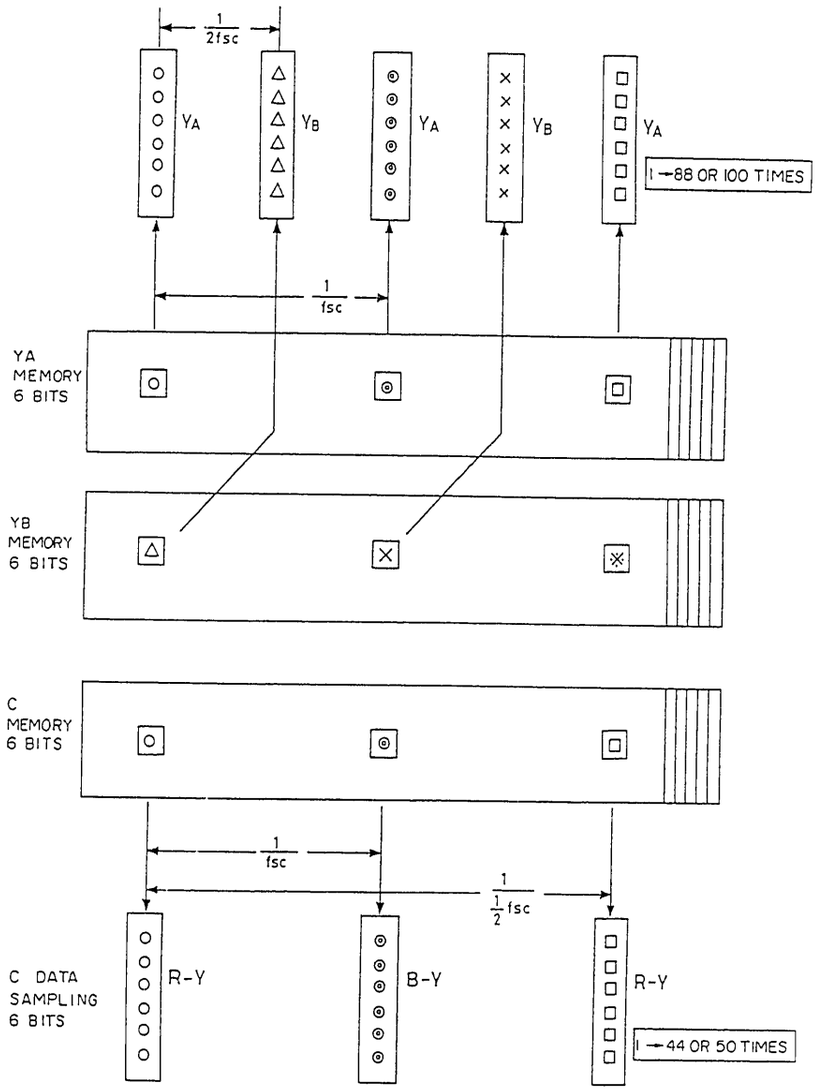


Fig. 3-16 Reading from Memory

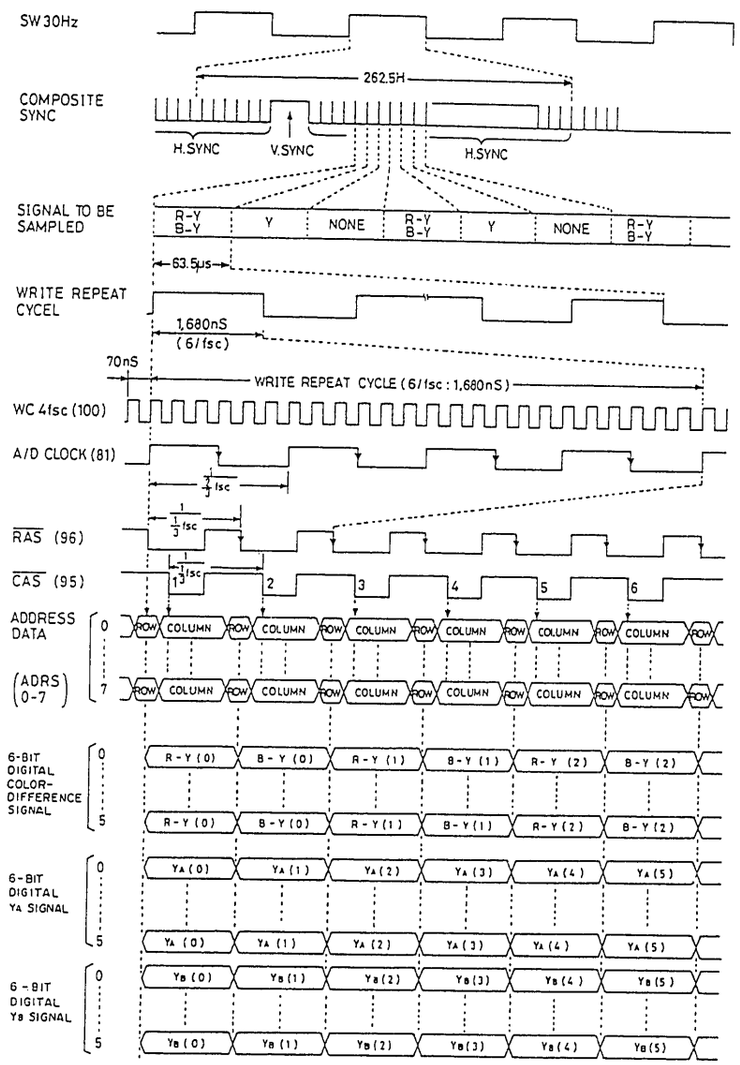


Fig. 3-17 Writing Timing Chart

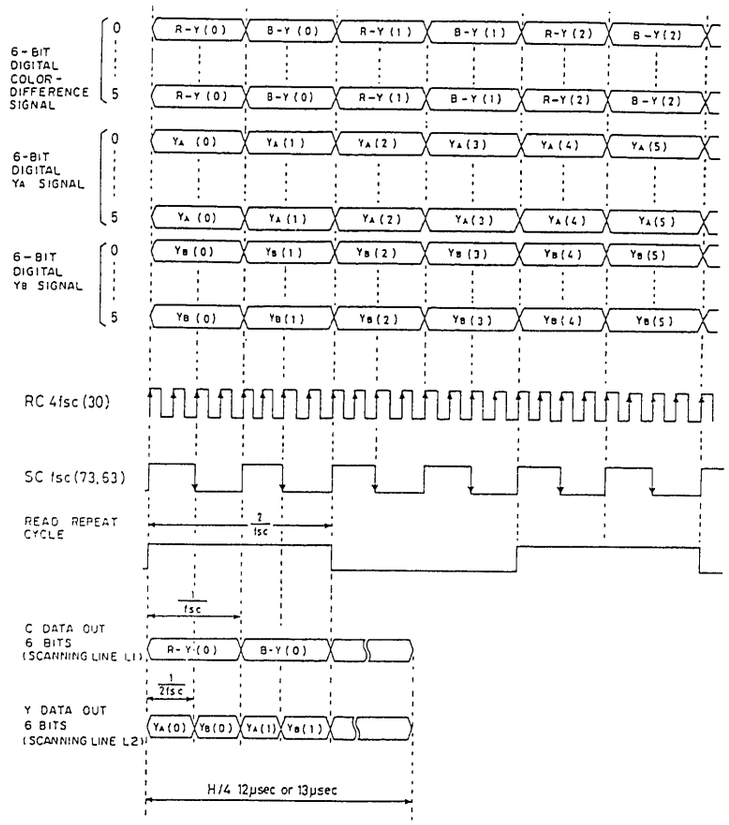

6-BIT DIGITAL COLOR-DIFFERENCE SIGNAL
6-BIT DIGITAL YA SIGNAL
6-BIT DIGITAL YB SIGNAL
R-Y(0) B-Y(0) R-Y(1) B-Y(1) R-Y(2) B-Y(2)
YA(0) YA(1) YA(2) YA(3) YA(4) YA(5)
YB(0) YB(1) YB(2) YB(3) YB(4) YB(5)
RC 4fsc (30)
SC fsc (73,53)
READ REPEAT CYCLE
C DATA OUT 6 BITS (SCANNING LINE L1)
Y DATA OUT 6 BITS (SCANNING LINE L2)
H/4 12μsec or 13μsec

Fig. 3-18 Reading Timing Chart

These are control signals to change the select switches of three signals, Y, R-Y and B-Y, and to DC clamp them. Figs. 3-11(c) and 3-13 show them in detail.

(f) BLP (pin 2)
This is a signal to control the OFF gates of the R-Y/B-Y demodulators. As described in chapter 5-2 (Figs. 3-10, 3-11(c)), this signal stops demodulation for approx. 12 μsec before and after A/D clamping to prevent external noise from entering.

(g) $\overline{RAS}$ (pin 96), $\overline{CAS}$ (pin 95), $\overline{WE}$ (pin 93), SC (pins 63, 73), $\overline{DT}$ (pin 94), ADDRESS 0 - 7 (Figs. 3-17, 3-18)
These are memory control signals the functions of which are the same as in P in P. As can be seen from Figs. 3-17 and 3-18, $\overline{RAS}$ designates row addresses. It designates the row addresses of the memory into which the picture information is written at the 1/3 fsc frequency. $\overline{CAS}$ is an output to designate column address. It designates the column addresses of the memory into which the picture information is written at the same frequency and also times writing. The digital picture information is written to the memory at the fall of this signal. $\overline{WE}$ is an output to control the writing of the picture information and its "Lo" output allows the writing enable mode. $\overline{DT}$ is a data transfer/read mode control output which determines the data output mode of the memory together with the $\overline{RAS}$ output. When the $\overline{DT}$ output goes "Lo" at the trailing edge of $\overline{RAS}$, the memory enters the data transfer mode, and when $\overline{DT}$ goes "Hi", the data read mode is entered. In the data transfer mode, 1H-component data on the memory cell array is transferred to the memory buffer. In the data read mode, the 1-H component data from the memory buffer is output for each bit (1 column), synchronized with serial clock SC (pins 63 and 73). SC is a clock output to read data from the memory. As can be seen in Fig. 3-18, it is a serial clock output, equivalent to fsc, that is necessary to read data on the line memory buffer in the memory. ADDRESSes 0 -7 are address data outputs of the memory as shown in Fig. 3-17 which are divided into rows and columns consisting of 8 bits

each. The picture data are written to the row and colum addresses in the memory according to the address codes designated at the fall of $\overline{RAS}$ and $\overline{CAS}$ respectively.

(h) MMQ (pin 25), MMT (pin 26)
(Fig. 3-19)
These are the picture horizontal display position adjustment input and output. The pulse obtained by delaying MMT output (pin 26) through external monostable multivibrator IC1013 is input to pin 25 (MMQ). The following describes operation of the picture display position adjustment circuit.

Since there may be scatterings of the picture display position on the left and right depending on the TV set used, both edges of multi pictures may be missed asymmetrically. To prevent this, a function to adjust the display positions of the multi pictures on the left and right is provided. This adjustment is done by the output of the monostable multivibrator (MM) determining the timing of the horizontal sync signal of the multi pictures. However, since the output time width of the MM is counted and used, counting may drift by one if the fall of the MM output fluctuates near the rise of the sampling clock. As this causes jitter in the displayed picture, it is necessary to take a countermeasure against the fluctuation of the MM. Fig. 3-19 shows the fluctuation countermeasure diagram. Two clocks are provided to count the MM output time width (2 fsc and 90° phase-shifted 2 fsc') and the clock that does not perform counting near the MM output edge is automatically selected, thus preventing the fluctuation of the counted values. That is, the circuit uses flipflops F1 and F2 and EX-OR G1 to detect that the fall of MM output is near the edge in the S1 Y output of the sampling clock. The output of flipflop F3 is inverted by the detection results and the sampling clock is switched to 2 fsc' that is phase shifted by 90°. This stabilizes the output of flipflop F4. Since 7.2 MHz (2 fsc) is selected for the sampling clock, the circuit can handle fluctuations of up to 35 nsec.

(i) EDGE OUT (pin 8)
This is the edge signal output. The EDGE signal is created from the edge outputs of the read column/row address generators and the output of gray back controller and is output from pin 8 to control the EDGE SW in IC1002. The gray back controller is responsible for controlling the sections of the 12 pictures not written to the overall edge level, that is, making them gray.

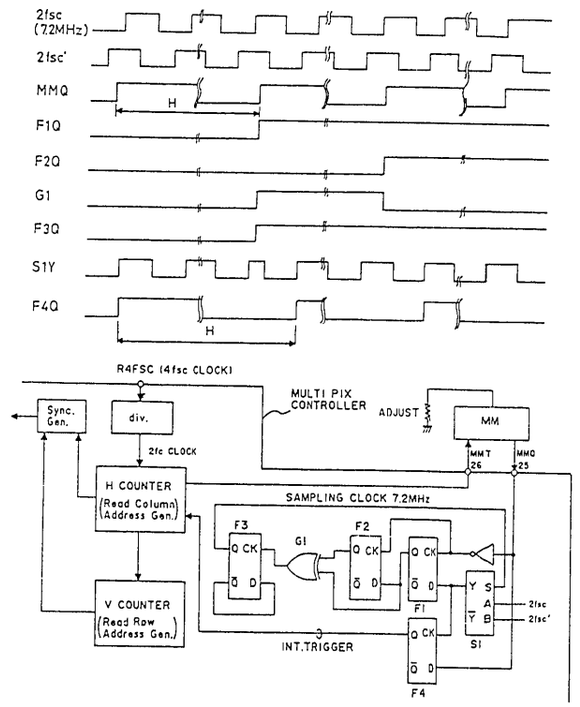


Fig. 3-19 Monostable Multivibrator Fluctuation Countermeasure Circuit

(2) Input processor (Figs. 3-15, 3-20)

The input processor receives the 6-bit digital video signals output from A/D converter IC1007 and converts them to digital signals, YA, YB and C (R-Y/B-Y), each consisting of 6 bits according to the memory configuration. The sampling frequency of Y is 2/3 fsc when totalling

YA and YB and is 1/3 fsc for individual YA and YB. The sampling frequency of C is 1/3 fsc when adding R-Y and B-Y signals and is 1/6 fsc for individual R-Y and B-Y signals.

C. LEVEL (pin 83) is a color-difference signal feedback clamp output. Since this is applied to pin 10 of MPX IC1009 to form a feedback loop, the clamp level of the color-difference signal is fixed precisely to 2.34V. The digital video signal input from the A/D converter is applied to the data separator which separates the signal into Y, C (R-Y/B-Y), each consisting of 6 bits. The Y signal is then serial-parallel converted and separated into YA and YB each consisting of 6 bits, then it is output to the memory. Meantime, the color-difference signal is a R-Y/B-Y time sharing synthesized signal and is output to the memory in the same way.

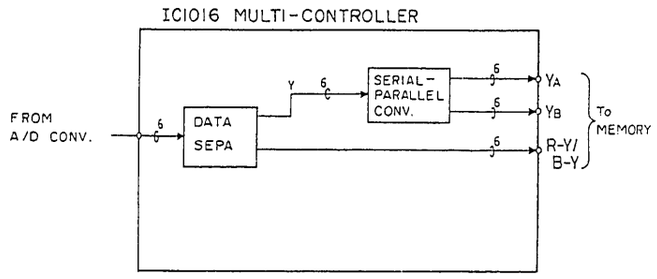


Fig. 3-20 Multi-Controller Input Processor

(3) Output processor (Figs. 3-16, 3-21 - 3-23)

Fig. 3-21 is a block diagram of the output processor. The YA, YB and R-Y/B-Y signals read from the memories are input to multi-controller IC1016, each consisting of 6 bits. YA and YB are parallel-serial converted in the reverse way to input processing to form a Y signal. Then a sync signal from the SYNC generator is added to the Y signal to create a digital Y signal. This addition is required because no sync signal is written to the memory in the multi-picture system.

The R-Y/B-Y signal is separated by the separator circuit to be the independent B-Y and R-Y signals each of which consists of 6 bits. Since no burst signal is written to memory in the chroma signal which is the same for the sync signal in the Y signal, the burst signal output from the SYNC generator is added to the B-Y signal. See Fig. 3-22 for the output signal waveforms up to here. The color-difference signals are converted by the next color encoder to a digital C signal.

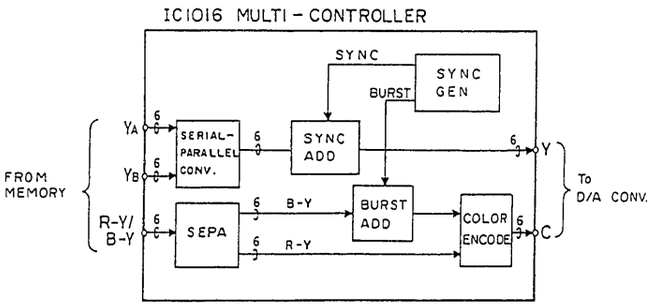


Fig. 3-21 Multi-Controller Output Precessor

Fig. 3-23 is a principle diagram of the digital color encoder. This encoder is the same as that built into P in P controller IC1017. The color-difference signals separated into R-Y and B-Y and the inverted -(R-Y) and -(B-Y) signals are produced. These four signals are quadrature modulated by the 4 fsc (14.3MHz) clock to produce an NTSC chroma signal.

The output of the encoder is applied to the D/A converter circuit as 6-bit digital chroma signals together with the Y signal.

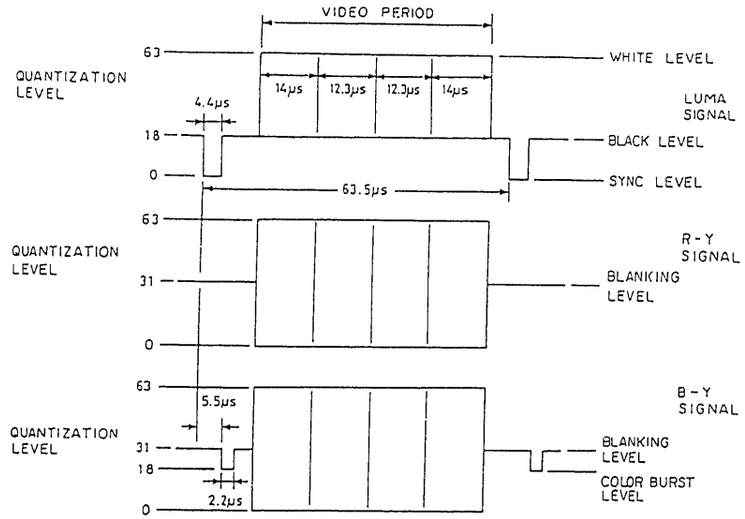


Fig. 3-22 Output Signal Waveform

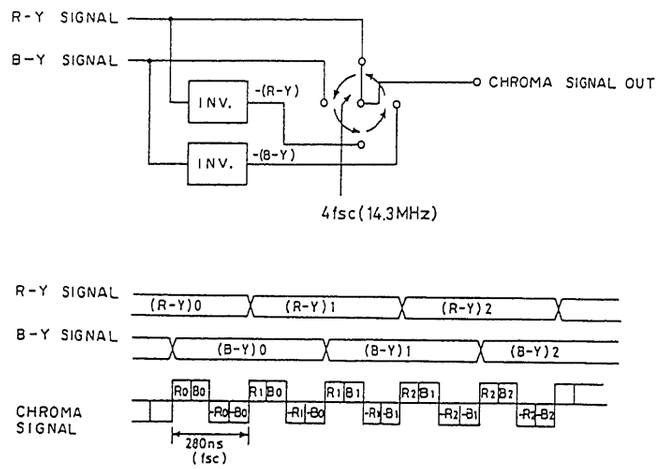


Fig. 3-23 Digital Color Encoder

3-5-4. D/A converter/YC mixer circuits (Fig. 3-24)

The digital Y and C signals output from multi-controller IC1016 are input to D/A converters IC1006 and IC1008 respectively. The frequencies of the clock signals are 4 fsc for both the Y and C signals. After each signal is R-2R type D/A converted, the Y and C signals pass through the 3MHz LPF and 3.58MHz BPA respectively and noise components in spurious bandwidths are reduced. The Y signal is directly supplied to the Y/C MIX circuit in Y/C MIXER IC1004, but the C signal bypasses the SUB BPF when the switch in IC1004 is set to the "Hi" side by the MULTI mode signal at pin 15 and is applied to the Y/C MIX circuit where they are mixed to form an NTSC signal and this is supplied to P in P switch IC1002. However, pin 15 is normally "Lo" in the P in P mode and the sub C signal passes through the gain controller for color level matching with the main C signal. When there is no signal in the main picture, pin 9 (MAIN SYNC) of IC1004 goes "Hi" and the internal switch is set to the NO VIDEO side, thus the gain controller is bypassed.

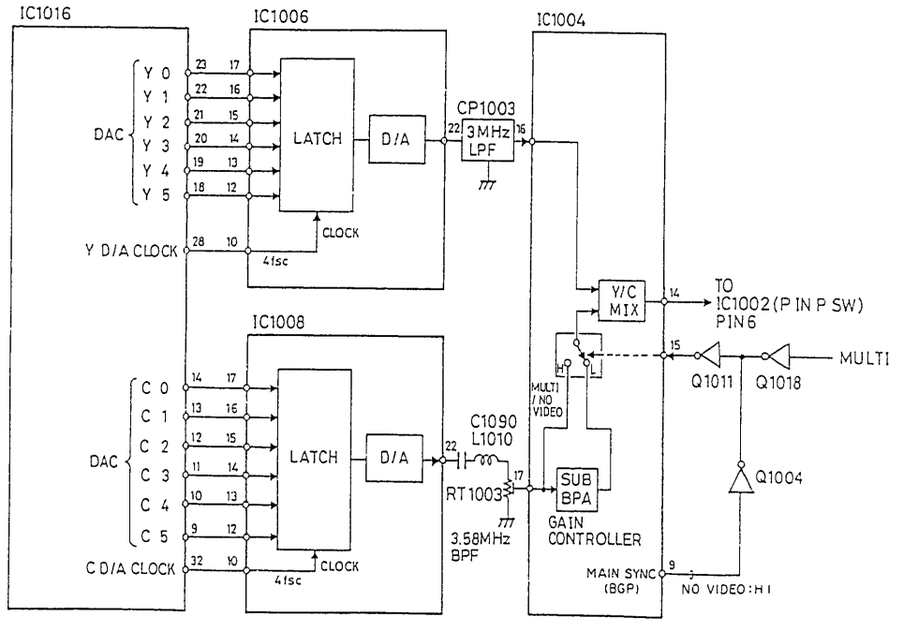


Fig. 3-24 D/A Converter/Y/C Mixer Circuits

3-5-5. Memory circuit (Fig. 3-25)

The multi-controller IC1016 is responsible for overall memory control and data communications in the multi-picture system. $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$, $\overline{WE}$ and SC are the control signals and ADDRESSes 0 - 7 are address data; their timing relations are shown in Figs. 3-17 and 3-18. The timing generator circuit in the memory receives $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$ and $\overline{WE}$ to control the column/row writing/reading timing. SC is input to the address counter to control the serial data read timing. ADDRESSes 0 - 7 are 8-bit address data; they output the row/column address data to the row/column decoders, timed by $\overline{RAS}$ and $\overline{CAS}$.

The memory cell array has 4 sheets of the memory field consisting of 256 columns x 256 rows and the four sheets correspond to input/output pins IO 0 - IO 3. IO 0 - IO 3 are used as the input pins to write the MPX video signals to the memories in this system. As can be seen from Fig. 3-6, 6 bits each of YA, YB and C, totalling 18 bits, are input to 16 bits in 4 ICs, IC1018 -IC1021, and to 2 bits, half of IC1022.

Since the frequency of the clock signal used for reading from the memory is three times (fsc) higher than that in writing, a serial output buffer is used. The data read from the memory cell array is transferred to the serial data selector through the transfer gate and data register, and the data the address of which is designated by the address counter is output to the serial output buffer. The signal from the serial output buffer consists of 6 bits of each YA, YB and C, a total of 18 bits, and is supplied to the MEM. VIDEO input pin group of multi-controller IC1016.

The memory map is as shown in Fig. 3-5. See Fig. 3-4 for the relationship with the displayed pictures.

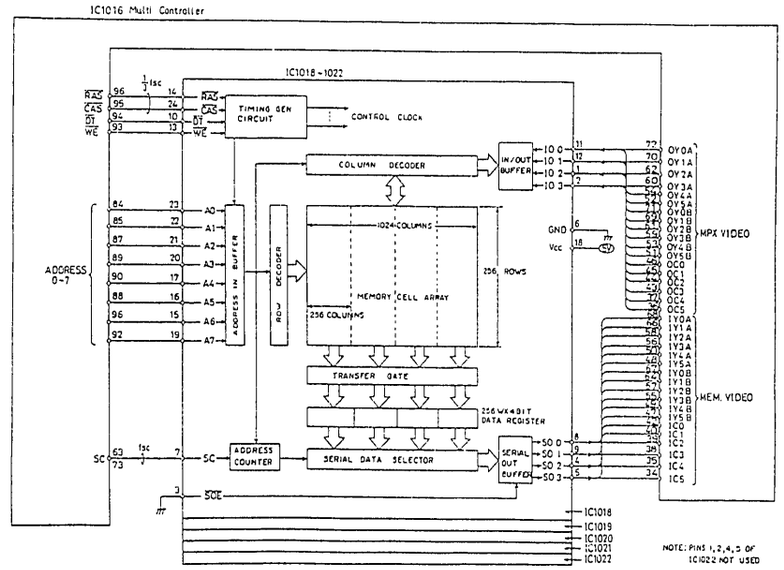


Fig. 3-25 Memory Circuit

3-5-6. Input/output switch circuit (Fig. 3-26)

The sub video signal in the multi-picture mode is selected by internal switch S6. S6 selects the PB video signal at pin 16 in the PB STROBO, SLOW STROBO, STILL STROBO and INDEX modes and the EE video signal at pin 14 in the EE STROBO and MULTI CHANNEL modes. The DC components are removed from these video signals by the coupling capacitors and the appropriate DC level is added to these signals by the bias circuit and clamp circuits in IC1002. The same can apply to the trick play video input at pin 20 and the sub video input at pin 6. The multi-picture video signal is applied to pin 6 as a sub video signal and is applied to P in P SW S2. S2 is fixed to the "Hi" side in the MULTI mode. S1 is an EDGE SW which is set to "Hi" at the edges of pictures, controlled by pin 8 of multi-controller IC1016, and outputs a gray edge level voltage, determined by the internal edge level. S1 output passes through the clip circuit (this circuit is used in the P in P mode) and amplified by the 8dB AMP to a video signal of 2Vp-p, then it is supplied to the LINE OUT jack and RF modulator.

Pin 7 P in P SW, pin 12 P in P INH and pin 21 trick play SW control circuit erase the pictures containing noise immediately after the MULTI mode is entered. See item 5-1 for details.

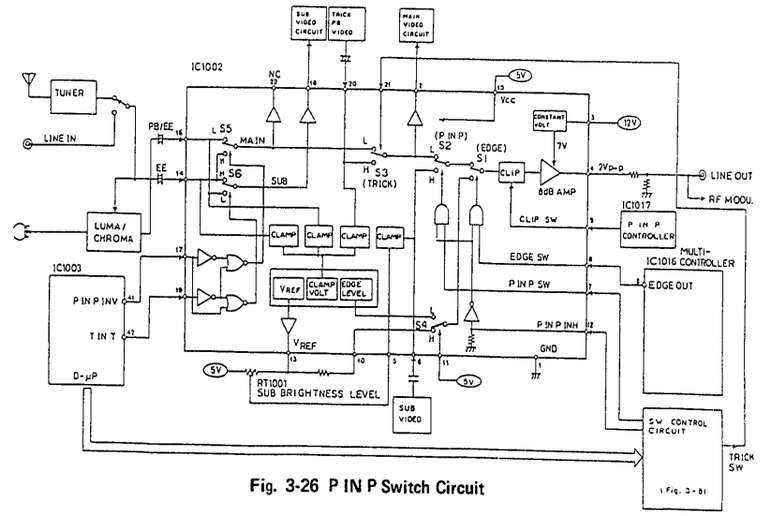


Fig. 3-26 P IN P Switch Circuit

TRICK PLAY

3-6. General Description

This VTR has a field memory which can store one field of the video signal for trick play, and this memory is utilized to reduce noise during trick play (still, search, slow, frame advance, strobo and recall) and in mode transitions and to upgrade performance. The recall function is newly added.

Table 3-51 shows specifications of digital trickplay.

Table 3-51 Specifications of digital trick play

Composition of heads	3 heads
Freeze	o
Strobo	o
Still	o
Slow	1/5 - 1/30
Frame advance	o
Search SP	o
EP	*
Recall	o
Paint, Mosaic	o
Processed signal	NTSC
Sampling frequency	3 fsc
Quantization	6
Composition of Memories	256K(dual port RAM)x4

* in search shows analog search not using the memory.

3-7. Video Processing Principles (Fig. 3-51)

Fig. 3-51 shows the principles of the video processing for trick play. The selected field of the composite video signal is sampled at 3 fsc and quantized to 6 bits, then it is serial-parallel converted to form 18-bit data consisting of three 6-bit units as one data unit with the rate of fsc. The 18-bit data unit consisting of three 6-bit data units is DPCM (Differential Pulse Code Modulation) converted and compressed to 16 bits to be stored in the 16 sheets of the field memory consisting of four 256-kbit DRAMs. Reading the video signal from the memory is processed by the reverse procedure to the above. When comparing the above with the system used in the previous model VT-1570A, the memories consist of 6 exclusive field memory ICs and one IC for sync signal totalling 7 ICs in the previous model VT-1570A, but in this model, they consist of 4 DRAM ICs. To reduce the memories in this way, serial-parallel conversion and DPCM processing are added to this model. The original picture is divided into 682.5 horizontal x 262.5 vertical. The horizontal 682.5 are obtained by dividing the 1 fH period by the rate of 3 fsc and the vertical 262.5 are scanning lines. The number of picture elements is 682.5 x 262.5 = 179,156. Since each picture element is quantized to 6 bits, the required memory capacity is 179,156 x 6 = 1,074,936. The actual memory capacity storing these is 256 x 256 x 4 sheets x 4 ICs = 1,048,576 which are not enough. Therefore, the 18-bit data unit consisting of three 6-bit data units is DPCM processed and compressed to 16 bits. This reduces the required memory capacity

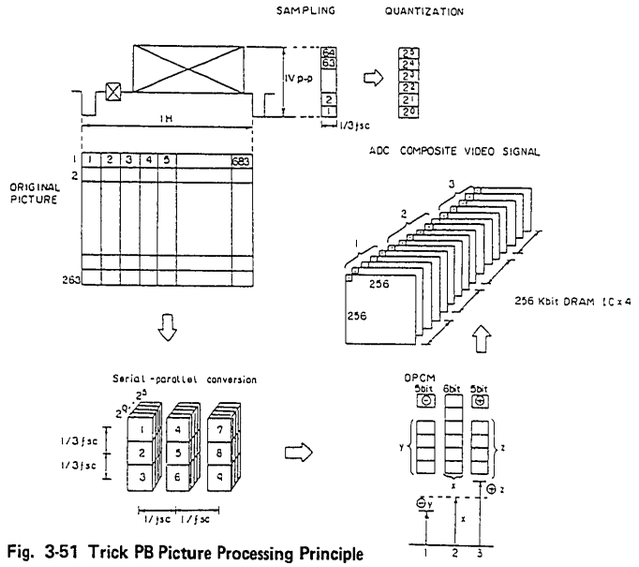


Fig. 3-51 Trick PB Picture Processing Principle

to 1,074,936 x 16/18 = 954,499 that can be stored in the memory provided.

Sampling is performed by dividing the composite video signal whoes maximum amplitude from the bottom of sync tip to the white peak is adjusted to 1V in 64 steps at the rate of 3 fsc. Quantization is performed by A/D converting this signal to 6-bit digital data. Since it is too fast to be stored in memory if sampling is done at the rate of 3 fsc, some measure must be taken to reduce the speed. To do this, three pixel data is handled as one unit to drop the rate to 1/3, that is fsc. Concerning the DPCM (Differential Pulse Code Modulation), from three components of data which were made in one unit in serial-parallel conversion (Assuming that pixels 1, 2 and 3 as shown by an example in Fig. 3-51), level x of data 2 at the center is quantized to 6 bits. Data 1 and data 3 on both sides adjacent to data 2 are expressed as a difference component from data 2. That is, if data 1 level is lower than data 2 level x by a component of y, 4 of the 5 bits are used to express y and the minus indication is given to the 5th bit. This 5th bit is called a code bit. If data 3 level is assumed to be higher than x by z in the same way, z is expressed by 4 bits and the code bit expresses plus. As described above, the DPCM compresses the 3 x 6 = 18 bits necessary to express 3 components of data to 16 bits to reduce the memory capacity, thus allowing the configuration of four 256-kbit DRAM ICs.

3-8. Use of Field Memory Output

The field memory output is utilized for the following three purposes.

- Digital video effect (freeze, strobo, mosaic, paint and recall)
- Picture hold in mode transition
- Noiseless trick play (still, frame advance, slow and search)

The operation principles of these modes are described in the following.

3-8-1. Freeze (Picture Still) (Fig. 3-52)

This is a picture still effect in which one-field video signal is stored in the EE or playback mode and is read repeatedly. In this mode, renewal of the field is stopped and sound is output. Fig. 3-52 shows the principle of using the field memory in the freeze mode. Vi shows the input of the trick play circuit and Vo shows the video signal output from the VTR. When the freeze mode is commanded in field F1, the video signal in the next field (F2) is written to the field memory (FIELD MEM) and is output simultaneously. In field F3 and later, the data in the FIELD MEM is read repeatedly until the freeze mode is released.

3-8-2. Strobo (Fig. 3-53)

When the SLOW SPEED UP button is pressed in the freeze mode, the strobo mode is entered. In the strobo mode, the video signals in new fields are stored at a certain interval and the freeze mode is repeated as can be seen in Fig. 3-53. This interval is determined by the digital μP (D-μP) to be set to 6 intervals, 2, 1, 0.5, 0.25, 0.125 and 0.0625 seconds. The interval is set to 2 seconds after the SLOW SPEED UP button is pressed in the freeze mode. These interval times can be selected by operating the SLOW SPEED UP/DOWN buttons.

3-8-3. Mosaic, Paint (Fig. 3-54)

The same data are repeatedly output in the horizontal and vertical directions in the EE or playback mode to provide a mosaic picture effect. Mosaicking the sync signal and burst signal is inhibited as shown in Fig. 3-54.

Since the continuity of the chroma signal must be maintained, data is output repeatedly in fsc units. When the D.V.E button is pressed, the mosaic mode is entered. Mosaics can be sizes, large or small, which are 8H/4 fsc and 4H/2 fsc in the vertical and horizontal directions. The size can be selected by operating the SLOW SPEED UP/DOWN buttons.

When the D.V.E button is pressed in the mosaic mode, the paint mode is entered. This mode provides an oil painting picture effect by fixing the lower 2 or 3 bits in the data of each pixel forcibly. Painting the sync and burst signals is inhibited in the same way as in the mosaic mode. Fixing 2 or 3 bits can be selected by operating the SLOW SPEED UP/DOWN buttons in the same way as in the mosaic mode.

When the D.V.E button is pressed in the paint mode, the VTR enters the mosaic + paint mode. One of 4 combinations of mosaic patterns, large and small, and paint bits, large and small, can be selected by operating the SLOW SPEED UP/DOWN buttons. Table 3-52 shows the above operations.

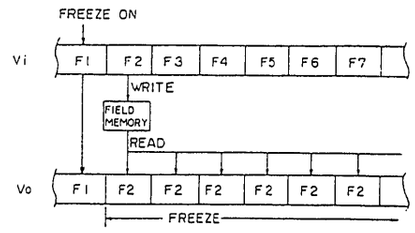


Fig. 3-52 Freeze

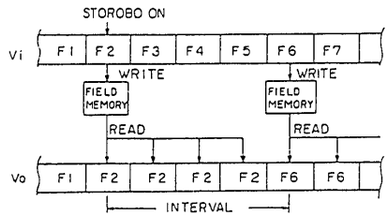


Fig. 3-53 Strobo

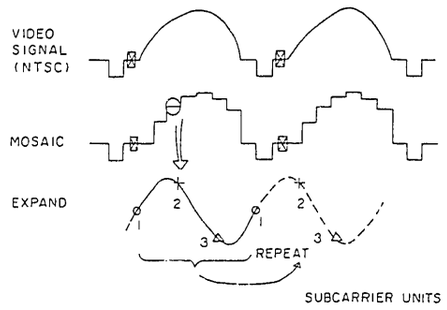


Fig. 3-54 Mosaic Effect

Table 3-52 Mosaic/paint mode operations

D.V.E. button operation	Mode	Slow Speed Up/Down button operation
Once	Mosaic	SS DOWN Mosaic small SS UP Mosaic large (initial state)
Twice	Paint	SS DOWN Paint small SS UP Paint large (initial state)
Third times	Mosaic + Paint	Mosaic small Mosaic small Paint small Paint large Mosaic large Mosaic large Paint small Paint large (initial state) SS UP SS DOWN
Four times	Normal	-----

3-8-4. Recall function (Fig. 3-55)

The field data stored last in the freeze, still and slow modes is read by operating the RECALL button after each mode is released as shown in Fig. 3-55. This function allows the picture to be printed when a video printer is connected to the VTR. The video signal is written to the memory in each of the above modes and the signal written last is read repeatedly by operating the RECALL button after the mode is released. This function is also effecitve in the multi-picture mode and is released in the P in P mode.

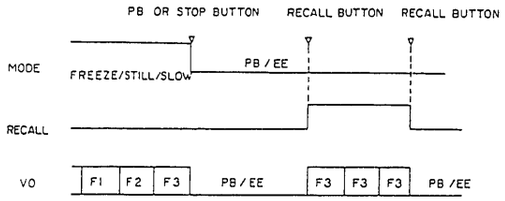


Fig. 3-55 Recall Function

3-8-5. Picture hold in mode transitions (Fig. 3-56)

When the mode is changed from play to forward/reverse search and vice versa, etc., the playback output contains a high level of noise, so the picture before the mode is changed is held until the mode transition is completed. Fig. 3-56 shows the principle of operation of the field memory during mode transition. When the FIELD MEM is commanded to select video

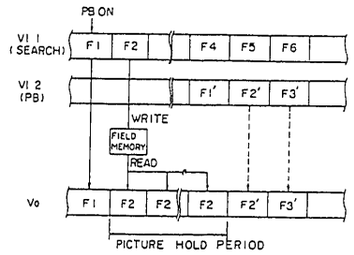


Fig. 3-56 Picture Hold During Mode Transition

signal Vi2 in field F1 while video signal Vil is output, it writes the video signal in field F2 and outputs it simultaneously. The video signal in the FIELD MEM is repeatedly read and output until video signal Vi2 is stabilized.

3-8-6. Trick play (Fig. 3-57)

In trick play modes such as still, frame advance, slow, etc., the field with least noise is selected and the video signal in the field is stored to replace the video signal in the field containing too much noise with it. The outputs of the three video heads installed in the upper cylinder are allocated in the modes shown in Table 3-53 and Fig. 3-57. The following are the uses of the field memory in each trick play mode.

VT-2805A has 4 video Head system, so please refer to VT-2600A Technical Information for 4 video Head system.

(Still)

Writing and reading are performed with the same timing as in the freeze mode described previously. The differences from the freeze mode are that the tape stops several frames after the video signal is written to the field memory and audio is muted. In this way, the video signal in the field with least noise is written and read. Therefore, a very clear still picture without jitter can be obtained.

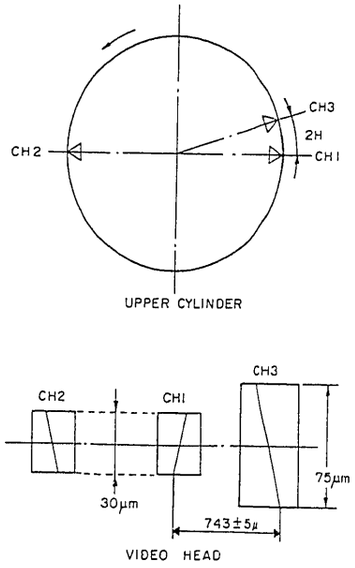


Fig. 3-57 Composition of Video Heads

Table 3-53 Allocation of video heads

OPERATION MODE	SP	EP
PB/REC	CH1/CH2	CH1/CH2
STILL	MEM(CH1 or CH2)	MEM(CH1 or CH2)
F. ADV	MEM(CH3)	MEM(CH2)
SLOW	MEM(CH3)	MEM(CH2)
SEARCH	MEM(CH1 & CH3)	CH1 & CH2

Note) MEM: The field memory is used.

(Slow/Frame Advance) (Fig. 3-58)

This VTR employs a SW30/CTL synchronization (PLL) slow playback driver which provides an accurate tape stop position and a short frame advance period to cope with the varible slow play and field memory. Fig. 3-58 shows the principle of operation of the field memory during 1/5 slow play. The one-field video signal just after the tape stops is stored in the field memory and is output simultaneously. After writing is completed, the video signal in the field memory is repeatedly read and output until the next frame advance is completed. In this way, a clear slow motion picture is obtained by simply controlling the tape stop position.

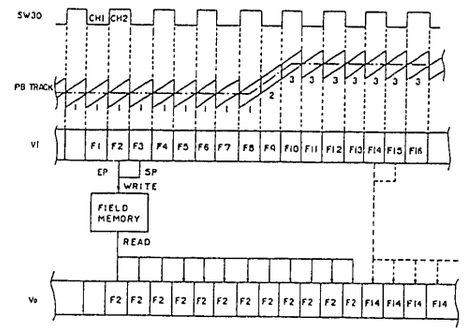


Fig. 3-58 Slow/Frame Advance Modes

(Search) (Fig. 3-59)

The field memory is used only for SP search. EP search is the same as in the previous VTRs. The video signals of one frame consist of the quantized playback output for the first field and the read output of the field memory which stores the quantized video signal in the first field for the next field. The playback output of one field consists of the partial playback outputs of three video tracks. To minimize jitter and noise among three video tracks, the CH-2 video track is traced by the CH-3 video head during a period of approx. 2/3 field and the CH-1 track is traced by the CH-1 head during remaining approx. 1/3 field. Switching of these heads is automatically commanded according to the comparison results of the CH-1 and CH-3 playback outputs. Fig. 3-59 shows the principle of the use of the field memory during SP search.

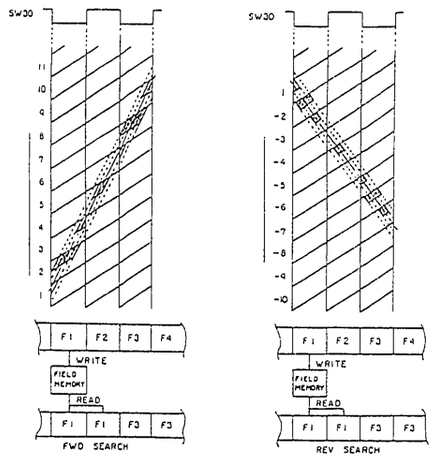


Fig. 3-59 SP Search Operation

3-9. Circuit Configuration (Fig. 3-60)

Fig. 3-60 is a block diagram of the video processing circuit for trick play and digital video effects. This circuit consists of the following blocks.

3-9-1. Digital µP (IC1003)

This is a system controller which controls the overall digital functions including P in P, trick play and multi-picture functions. It communicates data with the system control µP and timer µP and gives commands to the trick play controller (IC1015). The digital µP receives signals such as TRANSIENT, CM BRAKE, etc. as trick play functions and outputs mode signals including MOSAIC, PAINT, etc.

3-9-2. Trick play controller (IC1015) (Fig. 3-60 (a))

This receives the commands from the digital µP (IC1003) and controls the overall circuit as follows.

(1) Mode controller
This makes each internal block active and controls it when freeze, strobo, still, slow, frame advance, search, recall, paint or mosaic mode is set.

(2) Memory reference signal section
This supplies the MEMO. REF30 signal to PLL IC605 to generate a reference signal for controlling the cylinder phase.

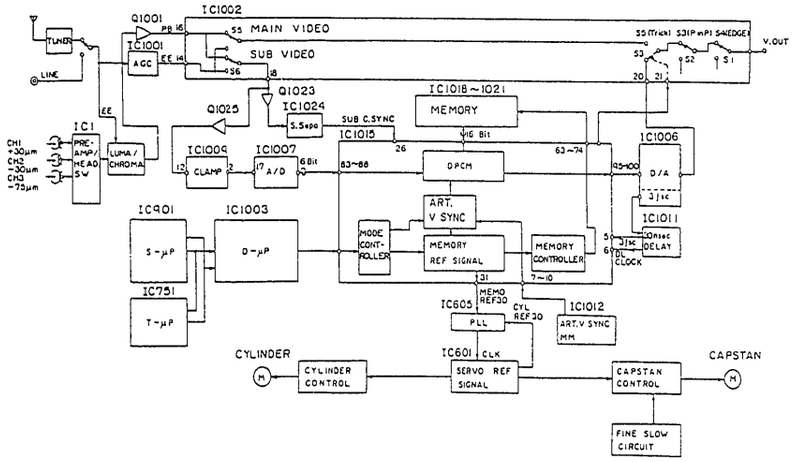


Fig. 3-60 Trick Play Circuit Block Diagram

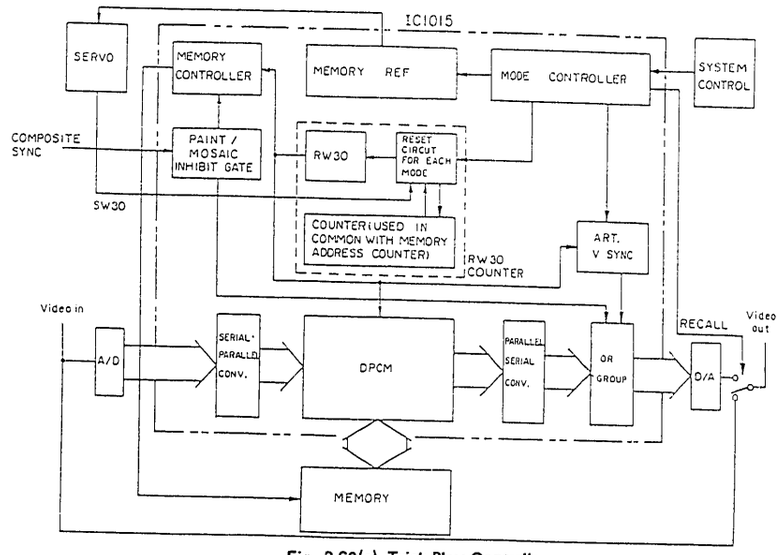


Fig. 3-60(a) Trick Play Controller

(3) Memory controller
This outputs address data consisting of 8 bits and memory controller signal of 4 bits to control writing and reading to/from the field memory (IC1018 - IC1021).

(4) Artificial V SYNC generator
This generates an artificial V sync signal during still, slow, frame advance and search to cancel sync distortion caused by missing of vertical sync signal and supplies it to the OR group circuit to add it to the digital video signal.

(5) DPCM
As was described in the principles of video processing, the DPCM (Differential Pulse Code Modulation) system is used to limit the required memory capacity and obtain the necessary picture quality with less memory ICs. (See Fig. 3-51)

3-9-3. Input/output switch (IC1002)

IC1002 is used in common by the P in P circuit. The video signal for trick play and digital video effects is selected by input switch S6 as a sub video output and is derived from pin 18. The video signal which underwent trick play/digital video effect processing enters IC1002 via pin 20 and its sync tip level is clamped, then the signal is selected by trick play switch SW3 and is output to the VIDEO OUT jack and RF unit.

3-9-4. Clamp circuit (IC1009)

This selects the video signal input to the A/D converter circuit and clamps it. Since the A/D converter is used in common for the P in P circuit described previously, it has two inputs, the signal multiplexed with the luminance and color-difference signals and the composite video signal. In modes other than P in P, the composite video signal is selected. The sync tip of the selected video signal is clamped to a voltage which is the same as the voltage that determines the minimum level of the A/D converter using a clamper. The switch control signal is supplied from the digital µP.

3-9-5. A/D converter (IC1007)

This samples the composite video signal using a clock signal, equivalent to 3 fsc, and codes it to 6 bits, thus converting it to a 6-bit digital composite video signal. This circuit is used in common for the P in P circuit. The clock signal necessary for A/D conversion is supplied from the trick play controller.

3-9-6. Field memory (IC1018 - IC1021)

This consists of four 256-kbit memory ICs each of which incorporates four sheets of the memory field composed of 256 x 256 bits. As described in the video processing principles (see Fig. 3-51), the 16 sheets of the memory field consisting 256 x 256 bits and 16-bit data units are stored in each address. The control signals for writing and reading and address data are supplied from the trick play controller.

3-9-7. D/A converter, clock signal generator (IC1006)

This D/A converts the digital video signal which was converted in reverse to DPCM and supplied from the trick play controller. The control signals necessary for conversion are supplied

from the trick play controller. IC1006 also generates a 3 fsc clock signal that is necessary for field memory control and DPCM conversion and supplies 3 fsc and delayed 3 fsc signals to the trick play controller through the 30nsec DELAY (IC1011).

3-9-8. 30nsec DELAY (IC1011)

Since only the clock signal, 3 fsc (93nsec), is not sufficient for the specification of the $\overline{RAS}$ access time of the RAM memory IC used in this model (100nsec minimum during "Hi"), a 30nsec DELAY circuit is added to supplement this lack. IC1011 delays 3 fsc applied from IC1006 by 30nsec and supplies it to the trick play controller.

3-9-9. REF30 PLL circuit (IC605)

This compares the phases of the REF30 signal that is obtained by dividing the fsc VCO output in IC605 by the main servo IC (IC601) and the main reference signal, MEMO. REF30, obtained from the memory reference signal section to correct the oscillation frequency of fsc VCO so that both signals are in phase.

3-9-10. SUB. SYNC SEPA. circuit (IC1024)

This receives the sub video signal from pin 18 of the P in P switch (IC1002) and separates a sync signal from it and then supplies this to pin 26 of the trick play controller IC as a sub composite sync signal. This becomes a reference signal for the paint inhibit gate and mosaic inhibit gate and for repeating data.

3-9-11. Artificial V SYNC monostable multivibrator (MM) circuit (IC1012)

IC1012 incorporates two MMs to determine the two time constants necessary for artificial V SYNC. One is the width of artificial V SYNC, approx. 6H, and the other is the variable delay time which can be varied by the V. LOCK control on the rear of the VTR. These two time constant signals are input to the trick play controller via pins 8 and 10 and is applied to the artificial V SYNC section.

3-9-12. AGC circuit (IC1001)

IC1001 is a keyed AGC circuit which functions in the P in P mode and keeps the amplitude of the TUNER or LINE IN EE video signal so that it is constant regardless of the variations in the input level for A/D conversion in the next stage. The output of this IC is applied to the EE input, pin 14, of P in P switch IC1002.

3-9-13. Head switching circuit (IC1)

As shown in Table 3-53, this selects the optimum playback outputs depending on the different modes and supplies them to the luminance/chroma circuit.

3-10. Circuit Operation

3-10-1. Digital µP (IC1003) (Fig. 3-61)

Fig. 3-61 shows the circuit responsible for trick play in the digital µP and its peripheral circuits which control the P in P and multi-picture functions as well as the trick play functions. Since

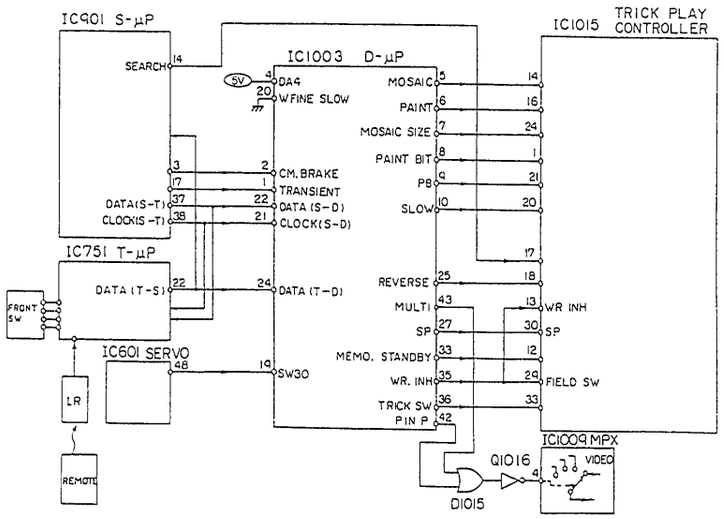


Fig. 3-61 Digital µP Circuit

digital µP IC1003 has a characteristic to expand the ports of the system control µP as described previously, it receives commands mainly from the system control µP and timer µP and decodes the serial data and supplies it to trick play controller to control it. Figs. 3-70 to 3-73 show the timing charts and the pin specifications are described in item 57-1.

(1) DATA (S-D), CLOCK (S-D), DATA (T-D) inputs
The system control µP and timer µP communicate data mutually through the 3-bit data bus of DATA (S-T), CLOCK (S-T) and DATA (T-S). These bus lines are also connected to the digital µP which can receive the commands from both µPs. DATA (S-D) is a data line from the system control µP to the digital µP, DATA (T-D) is a data line from the timer µP to the digital µP and CLOCK (S-D) is a clock signal which controls the timing of transmission and reception through these data lines.

As is shown in the Fig. 3-61, the operator's commands given by the front switches or buttons on the remote hand unit are transferred from the timer µP, and receiving them, the system control µp returns the data obtained every time the mode is shifted. See the system control for the communication timing charts and communication data in the system control circuit description.

(2) CM. BRAKE input
The capstan motor brake pulse is applied from system control µP IC901. This is necessary to determine the memory write timing in the still and slow modes and is provided as an independent port because this is not included in DATA (S-D).

(3) TRANSIENT input
The transient signal which goes "Hi" in mode transitions is supplied from the system control µP. This determines the switching timing of the trick play switch that switches the digital picture to the playback picture when still or slow is switched to play.

(4) DA4 input
There are DA 4-head and digital 3-head systems as the composition of Video Heads. This input selects them because the memory write timing, etc. are different depending on the video head system used.

(5) W. FINE SLOW input
This is set to "Hi" when the double fine slow in which the picture is stored for every field and appears in the DA 4-head mode or the single fine slow in which the picture is stored for every frame and appears when the digital 3-head mode is selected. This input goes "Lo" in other modes. This model uses a digital 3-head system and fixes the input to the GND so as to use a single fine slow function.

(6) SW30 input
This is a head switching signal supplied from the main servo IC601 which determines the memory write timing in the still and slow modes.

(7) MOSAIC, PAINT, PLAY, SLOW, SEARCH, REVERSE and SP outputs
These are the mode outputs which go "Hi" in each mode and "Lo" in other modes to expand the ports of the system control µP. However, the outputs of S-µP are directly used for SEARCH in this model.

(8) Mosaic size and paint bit outputs
As described in item 53-3, two types of both mosaic and paint can be selected. Table 3-54 shows the truth values. The mosaic size output is used in common with the P in P REV trick play output and goes "Hi" when the digital trick play is performed in P in P sub picture and goes "Lo" in other modes, but this function is not used in this model.

Table 3-54 Mosaic size and paint bit

Pins 7/8	Hi	Lo
Mosaic size	Large (8H/4 fsc)	Small (4H/2 fsc)
Paint bit	Rough (lower 3 bits fixed)	Fine (Lower 2 bits fixed)

(9) MEMO. STANDBY output
This is a control signal for the memory controller of the internal blocks of trick play controller. The "Lo" output makes the memory controller active and "Hi" disables it. However, the memory reference signal generator which supplies the MEMO. REF30 signal to the servo circuit continues to operate even in "Hi" mode.

(10) WR. INH output
This is a double-function output pin of WR INH and FIELD SW. The FIELD SW selects the head channels as shown in Table 3-55 depending on the composition of the video heads and tape speed so that the video output on the channel with less noise is stored in memory. Since this model uses a digital 3-head system, the FIELD SW selects channel 2 in EP, LP modes and channel 3 in SP mode.

Table 3-55 FIELD SW

Tape speed / Composition of heads	EP	LP	SP
DA 4	CH2	CH2	CH2
DIGITAL 3	CH2	CH2	CH3

The WR INH output is used to inhibit writing to the memory. "Hi" inhibits writing data to the memory and "Lo" allows writing. See Figs. 3-70 to 3-73 for the timing charts.

(11) TRICK SW output
This is a trick play mode output which sets trick play controller IC1015 to the trick play mode. "Hi" switches the output video signal to digital and "Lo" switches it to analog.

3-10-2. Input switch/MPX/A/D converter circuis (Fig. 3-62)

(1) Input switch circuit
In the trick play modes, both the T in T and P in P INV. signals supplied from D-µP to P in P SW IC1002 are "Lo" in order to connect internal switches S5 and S6 to the PB VIDEO input side. Both PB and EE video signals are coupled by the capacitors and the DC components are removed. In place of these, an appropriate DC level is applied to the video signal by the bias circuit and clamp circuit in IC1002.

The output of S6 is derived from pin 18 and applied to pin 12 (VIN) of MPX IC1009 through 3.58MHz LPA Q1025. The 3.58MHz LPA compresses the chroma signal to a low amplitude as a countermeasure against reducing the fidelity caused by high-amplitude signals in DPCM conversion described later.

(2) MPX circuit
The video signal input to pin 12 is precisely clamped by the outputs of the internal 1.84V GEN and 2.84V GEN so that the sync tip level is 1.84V and the white peak level is 2.84V.

This is the preparation for A/D conversion in the next stage. The clamped signal is selected by the MPX SW and is output at pin 2. MPX SW is controlled by the P in P and MULTI signals supplied from the D-µP. Pin 4 goes "Lo" in the P in P mode and MPX SW selects the B-Y, R-Y and Y signals. In the trick play mode, the P in P and MULTI signals go "Lo" and pin 4 "Hi" and the video signal is selected. The MPX output is applied to pin 17 of A/D converter IC1007.

(3) A/D converter
The COMPA/LATCH circuit latches the input at pin 17 and compared it with the V. REF GEN output and applies the comparison result to the 6-bit encoder. The V. REF GEN receives the outputs of 2V GEN and 3V GEN in MPX IC1009 and generates a reference signal obtained by dividing the dynamic range 1Vp-p into 64 steps to apply it to COMPA. The 6-bit encoder converts the latched COMPA output to a parallel data consisting of 6 bits and applies it to pins 88 - 83 (I0 - I5) of the trick play controller. The COMPA/LATCH and encoder are controlled by the A/D CLOCK signal supplied to pin 11 from the trick play controller.

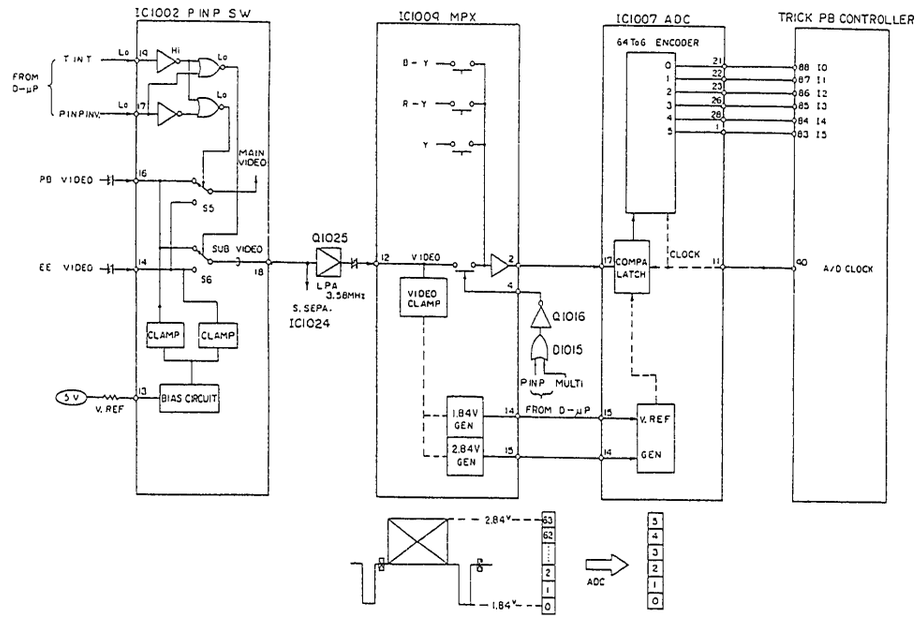


Fig. 3-62 Input SW/MPX/ADC Circuits

3-10-3. Serial/parallel converter/DPCM circuits (Fig. 3-63)

(1) Serial-parallel converter circuit
As has already been described in the principles of video processing, since it is too fast for the digital video signal to be written to the field memory at the sampling speed, 3 fsc, it must be dropped to 1/3, that is fsc. The serial-parallel converter is in trick play controller IC1015 and serial-parallel converts the 6-bit digital video signal with the cycle of 3 fsc output from A/D converter IC1007 to the 18-bit data with a frequency of fsc which is composed of three signals in one unit and stores it in the register in the next stage.

(2) DPCM circuit
As previously described in the principles of video processing, the 18-bit digital video data is compressed to 16 bits using the DPCM to reduce the number of memory ICs, so only 4 ICs are used while it is necessary to use 4-1/2 ICs without DPCM. Assuming that the data in the three components which are made into one unit are 1, 2 and 3, only data 2 (x) is expressed by 6 bits, and concerning data 1 and 3, the difference components with data 2, y and z, are expressed by 4 bits, and each remaining bit is used for the indication in the plus or minus direction as the code bit. This explains the composition of the DPCM video signal quantized to 16 bits. With the DPCM, data y and z consists of 4 bits each while data X is expressed by 6 bits, so only the difference 2 bits, that is the change up to 1/4 of data x can be expressed. In other words, when a step signal with the width of 1V is applied to A/D IN, the response at D/A OUT is in 2 steps as shown in Fig. 3-63. The step height of the approach is 1/4V and the width is 1/3 fsc, and 2 response timings can be considered, whether data 2 that is the reference has timing I or II.

However, it rarely occurs that the actual video signal is changed by more than 1/4 in one sampling cycle, and even if picture fidelity drops a little, it will cause hardly any problem in picture quality.

3-10-4. Memory reference signal generator circuit (Figs. 3-64, 3-65)

In the trick play/digital video effect modes, resetting when reading/writing to/from the memory is performed only every frame. Also, the rotation phase of the cylinder must be matched with the phase in reading from the memory. The memory reference signal generator generates reference signals to satisfy these conditions.

(1) Reference signals for reading/writing
The signals to be reference for reading/writing are provided in the blanking period of the video signal and are different in each mode as shown in Table 3-56.

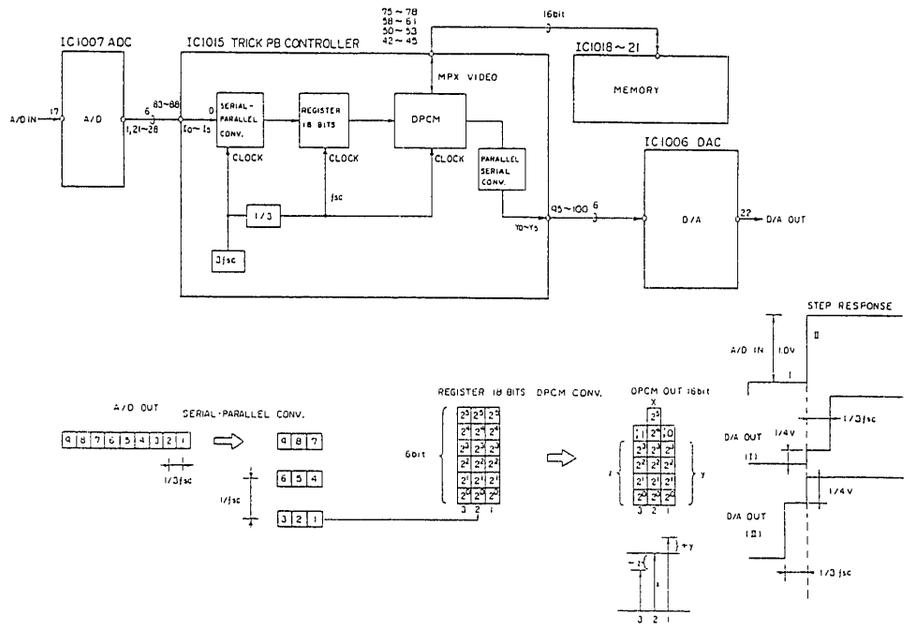


Fig. 3-63 Serial-Parallel Converter/DPCM Circuits

(a) The vertical sync (V SYNC) signal is used in the EE modes such as EE freeze and strobo modes.

(b) The reference signal (RW30) produced by the memory controller is used in the still, slow, play recall and play freeze modes. In these modes, the frequency of SW30 varies because of intermittent driving or mode transitions. Therefore, if SW30 was used as a reference signal for reading/writing, the field length would vary resulting in jitter and skew in the vertical direction. To prevent this, a reference signal which shows the lock point of SW30 in normal state of every mode is formed and is used as RW30 in the following cases.

- Writing in the state when the cylinder is rotating stably (SW30 and RW30 coincide)
- Reading during intermittent driving and mode transitions (SW30 and RW30 do not coincide)
- Writing in the state when the cylinder rotation becomes stable again (SW30 and RW30 coincide again)

(2) Servo synchronization

To create RW30, the memory controller and played back video signal (servo controller) must be synchronized. Fig. 3-64 shows a block diagram of the servo synchronization circuit and the timing chart.

(a) PLL IC605 compares the phases between the cylinder phase reference signal (CYL REF30) and memory reference signal (MEMO. REF30) and feeds back the comparison result to the clock signal input of the servo controller in IC601 to synchronize these two loops.

(b) A counter which operates at the same period of cycle as the MEMO. REF30 is provided for the memory controller in IC1015 and is reset by SW30 in modes other than slow, recall, freeze and transient.

(c) Since the counter operates at the same period of cycle as MEMO. REF30 after the reset is released during slow, recall, freeze and transient, the lock point of SW30 is indicated as long as MEMO. REF30 and CYL. REF30 are phase locked.

RW30 is created by the above operations.

(3) Continuity of H SYNC

Trick play using the field memory can be considered as a system that one-field video signal is output repeatedly, and at this time, the continuity of H SYNC is important.

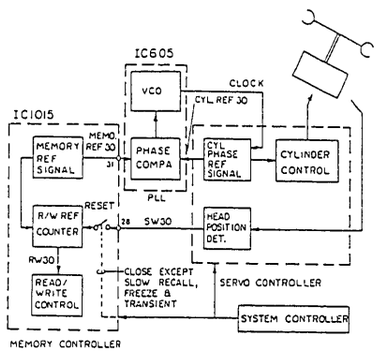
During trick play, the video head trace pattern becomes as shown in Fig. 3-65 (A) as opposed to that during normal play and the number (H) of H SYNC pulses in a field is obtained by the following equation.

$$H = 262.5 + (10n) \times \text{alpha H}$$

Here, alpha H is 1.5 in SP and 0.5 in EP and

n (multiple of speed):

Forward double speed	n = 2, 3, 4 ...
Normal play	n = 1
Still	n = 0
Reverse double speed	n = -1, -2, -3 ...



Block Diagram

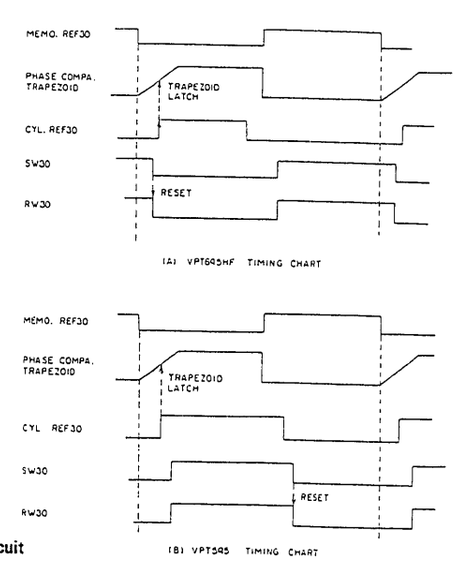


Fig. 3-64 Servo System Synchronization Circuit

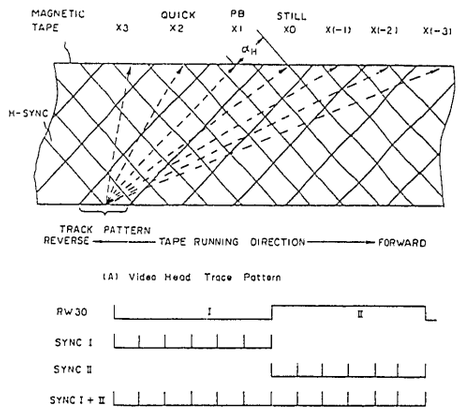
As can be seen from the above equation, it is divided into two ways as follows.

When n is an even number (including n = 0),
H = m (m is a integer)
When n is an odd number, H = m + 0.5.

(a) When n is an even number, the explanation is given using Fig. 3-65 (B). When the cycle period of RW30 I and II are made the same as in writing, the number of H SYNC pulses in the read signal is m as shown by SYNC I and SYNC II. Therefore, the continuity of SYNC I and SYNC II becomes SYNC I + II and the H SYNC is continuous.

(b) When n is an odd number, the explanation is given using Fig. 3-65 (C). When the cycle period of RW30 I and II are the same as in writing in the same way as in (a), RW30 and REF30 I/II are shown in i). There are (m + 0.5) number of H SYNC pulses in RW30 I and II. So, if the start of the read signal matches H SYNC, it ends at the half cycle point of H SYNC, resulting in SYNC I, II.

When these two fields are joined, H SYNC becomes SYNC I + II and discontinuity occurs. Therefore, RW30 I is read as a length of m and RW30 II is read as a length of (m + 1). In this case, number m of H SYNC (SYNC 1) is contained in RW30 I and number (m + 1) of H SYNC (SYNC II) in RW30 II as shown in ii). When these are joined, H SYNC is continuous as shown by SYNC I + II. When n is an odd number, RW30 in one-frame unit must be considered. (In the block diagram shown in Fig. 3-64, the counter reset pulse in the memory controller is to be 30Hz and the length of one field is set by the counter value in each mode.)



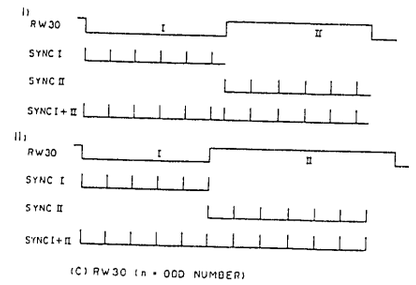


Fig. 3-65 H SYNC Continuity

3-10-5. Memory control circuit (Figs. 3-66, 3-67)

Fig. 3-66 is a block diagram of the memory control circuit. The trick play memory group consisting of IC1018 to IC1021 is controlled by $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$, $\overline{WE}$ and address outputs A0 - A7 applied from trick play controller IC1015 and SC applied from multi-controller IC1016. $\overline{RAS}$ designates the read timing of the row address and $\overline{CAS}$ designates that of the column address. $\overline{DT}$ designates the mode in which data is read from the memory to the controller and $\overline{WE}$ designates the mode in which data is written from the controller to the memory. SC is a clock signal to output the memory data serially in the multi-picture mode. Fig. 3-67 shows the timing chart of this circuit.

The 3 fsc signal produced by IC1006 is inverted by IC1011 and is applied to pin 5 of IC1015 where it is divided by 3 by the 3-phase shifter. IC1011 incorporates a 30nsec delay circuit consisting of C and R and the 3 fsc signal delayed here is applied to the memory controller as a delayed clock (DLC). This DLC is necessary due to the performance of the memory. The minimum time required for the "Hi" period of $\overline{RAS}$ in the memory is 100nsec, but the clock signal, 1/3 fsc, provides only 93nsec and does not satisfy the specification. Therefore, the signal delayed by 30nsec is used together to produce $\overline{RAS}$, thus satisfying the specification. Both $\overline{RAS}$ and $\overline{CAS}$ have a cycle time of 1/fsc and become the trigger signals to accept the row address and column address at their trailing edges when addresses A0 - A7 indicate row address and column address. When $\overline{DT}$ and $\overline{WE}$ are "Hi", the read/write inhibit states are entered and these instructions are given from the write timing block through the gate circuits. The 16-bit data is read and written from/to 4 memory ICs at the trailing edges of $\overline{DT}$ and $\overline{WE}$. The address signals are counted by the address counter at the fsc clock for row and column operations and are applied to

the memory ICs as 8-bit data through the address selector. The address selector switches the address data between the read and write modes and outputs it. This switching signal is supplied from the memory controller. The row counter receives the carry from the column counter as a clock signal. SW30 from pin 28 during play or the reset output of RW30 GEN during slow is selected by S1 and S2 and applied to both counters as a reset signal. The counters are reset by the vertical sync signal in the input video signal in modes other than play.

The WR. INH signal at pin 13 that is input to the write timing circuit is supplied from pin 35 of digital μP IC1003 as an instruction designating the timing at which the video signal written to the memory as shown in Figs. 3-70 - 3-73 timing charts. The FIELD SW (pin 29) is a control input which selects the CH1 or CH2 field of the picture in which noise is less in the slow and still modes. IC1018 - IC1021 are dual port DRAMs each of which has 4 sheets of the memory area consisting of 256 x 256 bits. The timing signal generator circuit receives $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$ and $\overline{WE}$ and generates a control clock signal and a strobe pulse to control the overall memory operation. The address input buffer section receives an address strobe pulse from the timing signal generator and accepts 8-bit row or column address data and then outputs it to the row/column decoders and address counter for serial output. The row/column decoders designate the address in the memory area from or to which data is read or written according to the row/column address data. The input/output buffer is a buffer register which outputs the data read from the memory cell array through the column decoder to the trick play controller or writes the digital video signal supplied from the trick play controller to the memory cell array. These memory ICs also have the serial output ports and serial operation is possible together with the RAM ports described previously. These serial ports are used in the multi-picture mode and were described in detail previously.

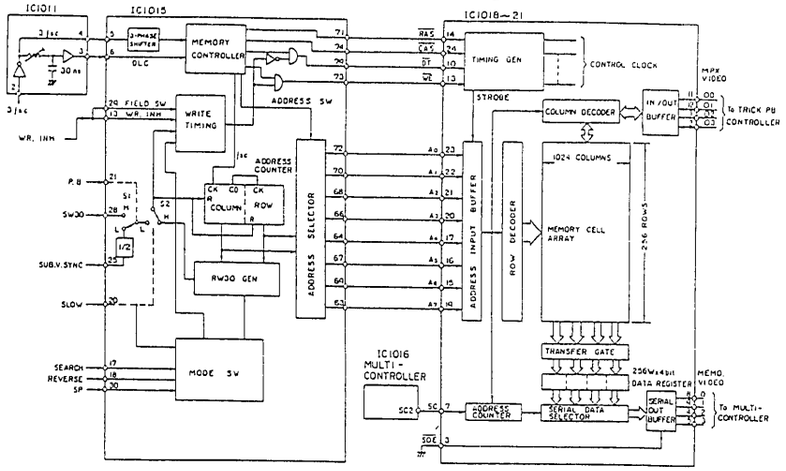


Fig. 3-66 Memory Control Circuit

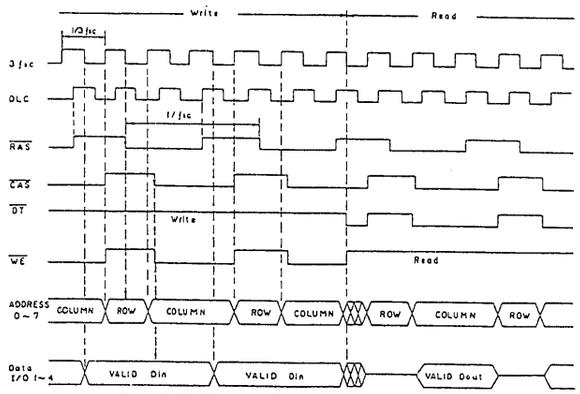


Fig. 3-67 Memory Control Circuit Timing Chart

3-10-6. Artificial V SYNC circuit (Fig. 3-68)

During trick play, V SYNC in the video signal is erased and new V SYNC (artificial V SYNC) is added because (A) the signal deterioration around V SYNC is conspicuous and (B) non-interlacing is provided as the same signal is read repeatedly (if it was interlaced, it would be seen as jitter in the vertical direction), etc. The artificial V SYNC signal is produced by making the edge of RW30 (start of the output video signal) as a reference. Therefore, there are two types of RW30 involved in the continuity of H SYNC.

(1) RW30 when n is an even number
The length of one field set by RW30 becomes an equal interval. Therefore, when artificial V SYNC is added with a fixed phase from the edge of RW30, a non-interlaced picture is obtained.

(2) RW30 when n is an odd number
The one-field length set by RW30 varies for every field. Therefore, if artificial V SYNC is added with fixed phase from the edge of RW30, the picture has vertical jitter. The fixed delay and variable delay are provided for RW30 as shown in the timing chart in Fig. 3-68 and the position of artificial V SYNC is adjusted by the variable delay, thus the picture non-interlaced.

The amount by which the position of artificial V SYNC must be adjusted is different depending on the TV and it is difficult to fix it at present.

The delay circuit consists of two monostable multivibrators in IC1012. MM1 determines the variable delay amount adjusted by the V. LOCK control and MM2 determines the width of artificial V SYNC, approx. 6H.

Pin 22 is a main video H SYNC input and SHIFT at pin 40 shifts the position of artificial V SYNC by 1/4H with respect to the edge of H SYNC if necessary becasue the virtical jitter may appear when sync separation is performed digitally in a digital TV.

The artificial V phase block receives a RW30 signal and generates a trigger timing signal for the internal fixed delay pulse and variable delay pulse from the leading and trailing edges of RW30 and outputs it to the artificial V SYNC block. The mode block selects these fixed/variable delay pulses depending on the modes as shown in Table 3-56.

The artificial V SYNC signal produced by the the artificial V SYNC block as above is added to the digital video signal in the OR circuit.

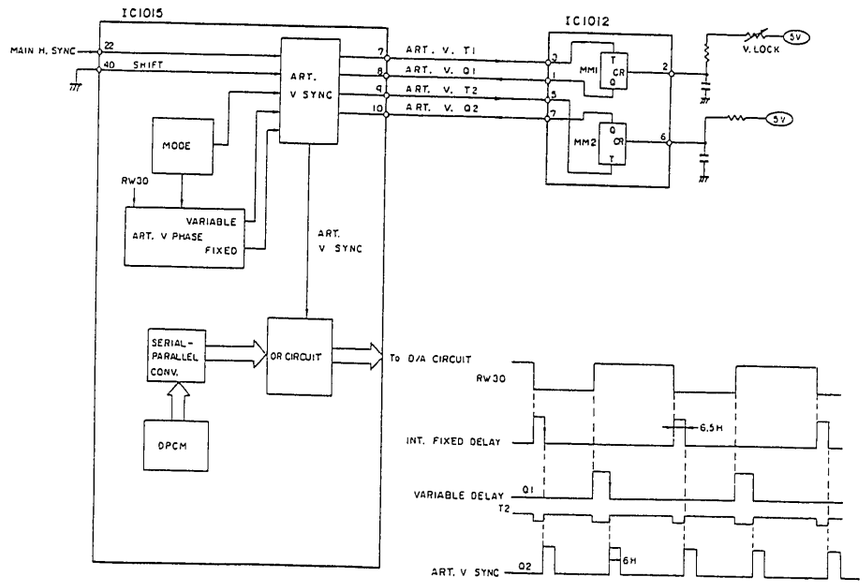


Fig. 3-68 Artificial V SYNC Circuit

Table 3-56 List of read/write reference signals and artificial V SYNC signal

		Read/write reference signal	No. of H SYNC in a field	RW30 field Length CH1/CH2	Artificial V SYNC
EE RECALL, EE FREEZE, EE STROBO		V. SYNC	262.5	262/263	Variable
PB RECALL, PB FREEZE, PB STROBO		RW30	262.5	262/263	Variable
SLOW, STILL	SP	RW30	262	264/264	Fixed
	EP		263	263/263	

3-10-7. Parallel-serial converter/OR block/D/A converter output switch circuits (Fig. 3-69)

The digital video signal read from the memory in the various trick play/digital video effect modes is 16-bit to 18-bit converted by the DPCM block in the reverse way to writing and is applied to the parallel-serial converter circuit in the next stage. The parallel-serial converter performs the reverse conversion to serial-parallel conversion during writing and converts the 18-bit digital video signal with a 1/fsc cycle time to three 6-bit digital video signals with a 1/3 fsc cycle time. The LOAD signal, fsc, is supplied as an output of internal switches S7 and S7 normally receives fsc from the memory controller. In the mosaic mode, S7 is switched to the "Hi" side and reads the same data repeatedly for the 2 or 4 fsc period depending on the mosaic size designated by pin 24. The D.V.E INH block controls S7. This circuit inhibits paint and mosaic processing during the blanking period. (The processing in the vertical direction of the mosaic effect is performed by the write timing block.)

The OR block in the next stage adds the artificial V SYNC signal to the signal output from the parallel-serial converter and it also processes the paint effect.

The lower 3 or 2 bits of the 6-bit digital signals are fixed, designated by the PAINT BIT signal applied to pin 1. The output of the OR block is applied to D/A converter IC1006.

The 6-bit digital video signal applied to D/A converter is latched according to D/A clock signal DACK (pin 10) and is D/A converted by the R-2R type D/A circuit in the next stage.

The D/A converted video signal, with unnecessary high-frequency components removed by 4.5MHz LPF CP1002 and buffer Q1006, is applied to the trick play input, pin 20, of P in P switch IC1002.

The trick play video signal input from pin 20 or main video signal is selected by the control signal (pin 21) at S3 in IC1002. The diode OR signal of TRICK PLAY or MULTI is input to pin 21 and the signal at pin 20 is output in these modes. A clamp voltage of approx. DC 2V is applied to pin 20 by the internal clamp circuit.

S2 and S1 in the next stage are P in P SW and EDGE SW respectively. Both are set to the "Lo" side and applies the trick play video signal to the 8dB output amplifier. The video signal amplified by 8dB is divided by the external resistors connected to pin 4 to be 2 Vp-p and is supplied to the LINE OUT jack.

3-11. Timing Charts

(1)	FREEZE, MEMORY RECALL	Fig. 3-70
(2)	SINGLE STROBO	Fig. 3-70
(3)	MOSAIC, PAINT, MOSAIC + PAINT	Fig. 3-71
(4)	MOSAIC/PAINT + -	Fig. 3-71
(5)	PB - STILL (F.ADV) - PB	Fig. 3-72
(6)	PB - SLOW - PB	Fig. 3-73

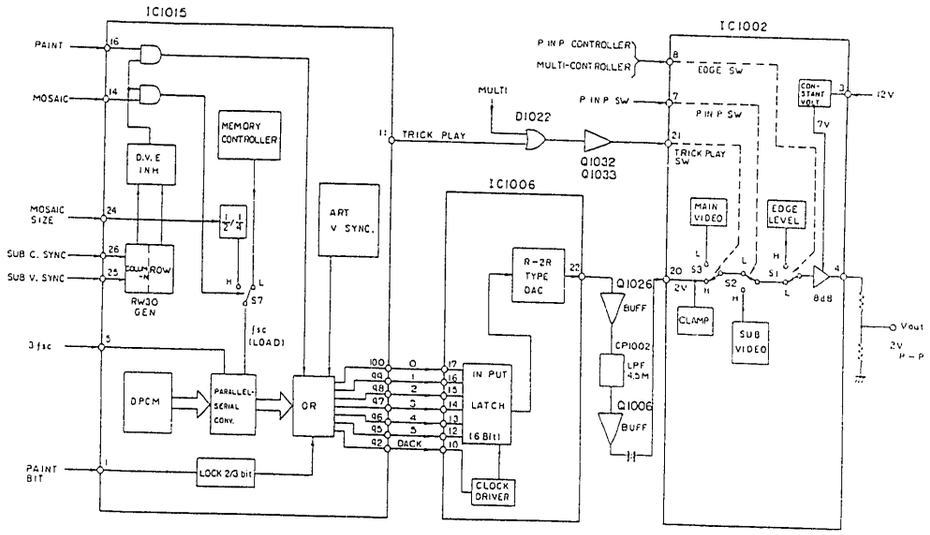
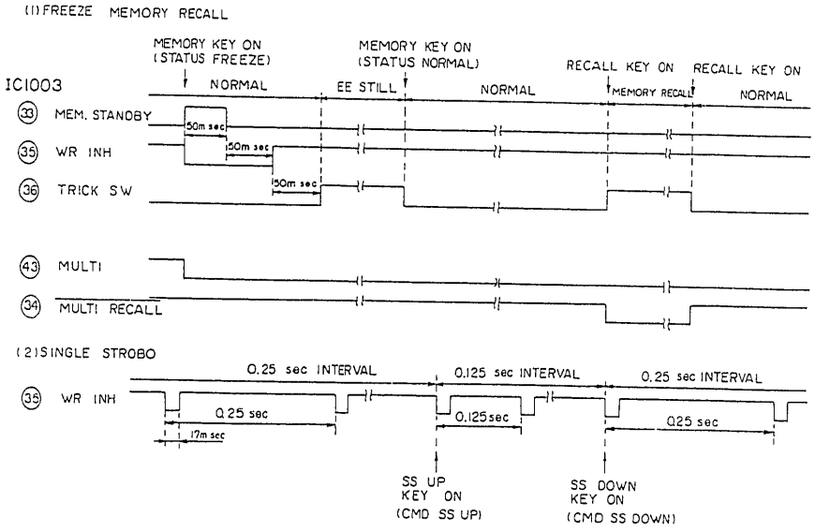


Fig. 3-69 Parallel-Serial Converter/OR/DA Converter/Output Switch circuit



There are 6 interval times — 2 sec, 1 sec, 0.5sec, 0.25sec, 0.125sec, 0.0625 sec.

INITIAL INTERVAL

When SS-UP/DOWN Key is held for 0.8 msec or longer, 1 step up/down is performed for every 0.8 msec.

Fig. 3-70 Timing Chart (1/4)

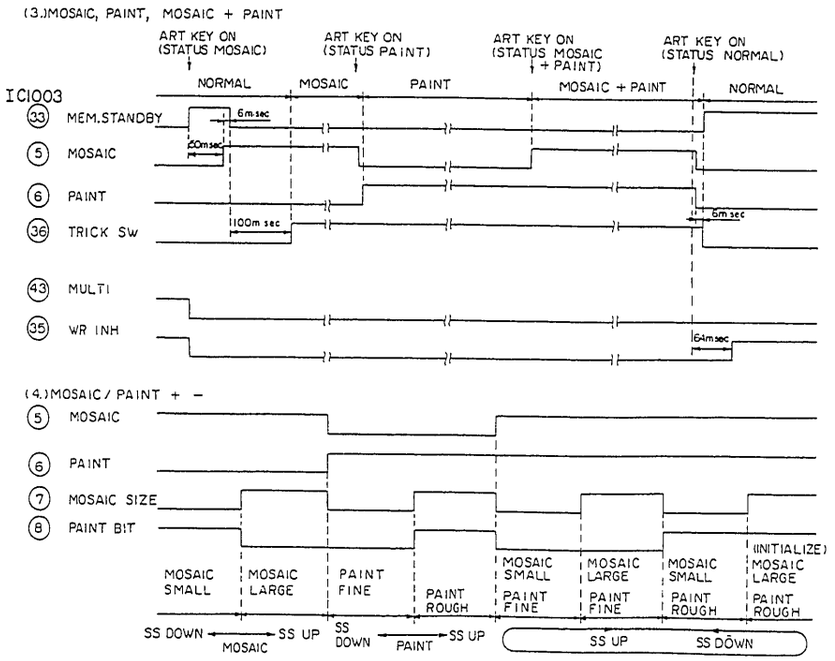


Fig. 3-71 Timing Chart (2/4)

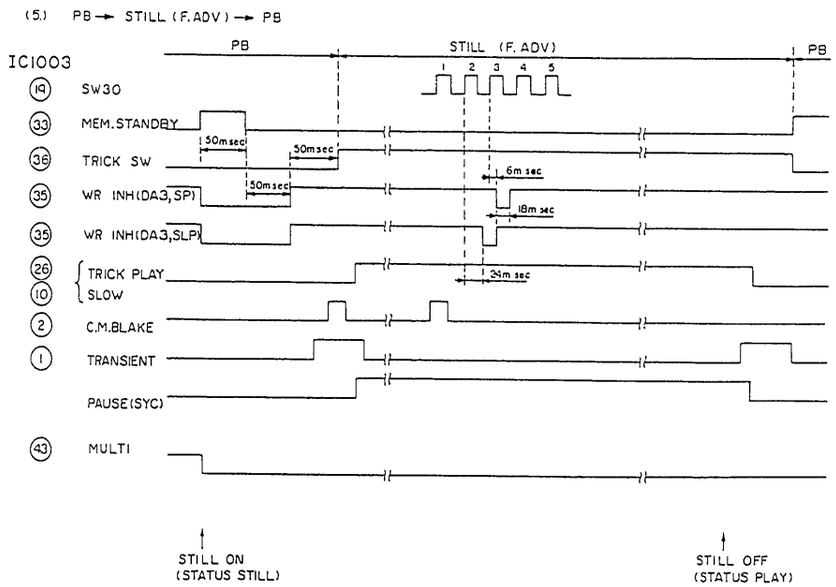


Fig. 3-72 Timing Chart (3/4)

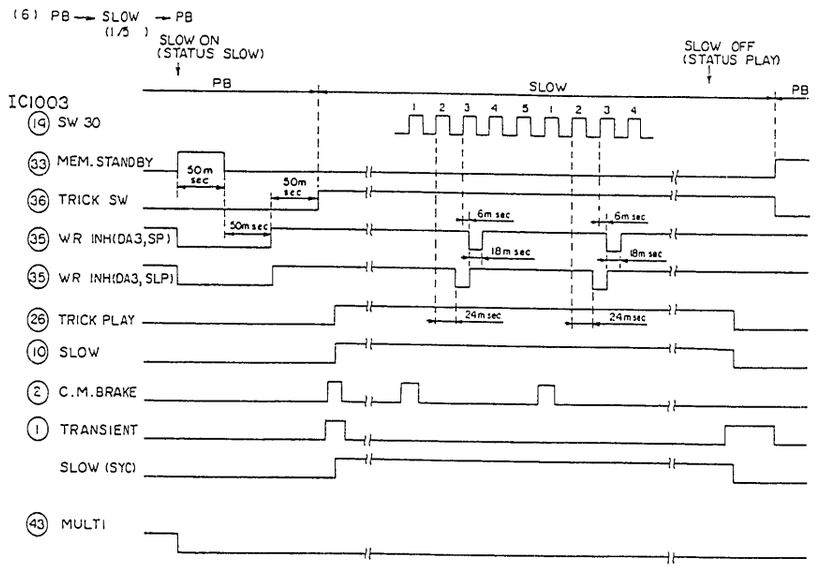


Fig. 3-73 Timing Chart (4/4)

P in P CIRCUIT

3-12. General

The P in P function allows framing a sub-screen reduced to approx. 1/9 the main screen in area in one of four corners of the main screen and displaying a picture other than the main picture in the sub-screen. In this mode, the configuration of the pictures is different according to the VTR mode as shown in Fig.3-101; it is called P in P in the play mode and T in T during stop, fast forward and rewind. In the record mode, this function is inhibited. The trickplay pictures such as search, slow, etc. are displayed only in the sub-screen.

VCR MODE	P in P	P in P Inversion	LINE / TUNER SW
STOP F.FWD REW	LINE (LINE)	LINE (LINE)	LINE
	TUNER (LINE)	LINE (TUN-ER)	TUNER
(NO SIGNAL) (OF LINE) STOP F.FWD REW	TUNER (BLACK)	BLACK (TUN-ER)	TUNER
	INHIBIT	INHIBIT	LINE
PLAY	PLAY (EE)	EE (PLAY)	EE
REC	INHIBIT	INHIBIT	EE

NOTE : EE=LINE OR TUNER

Fig. 3-101 Monitor Output Mode in P in P

3-12-1 Sub-screen video processing principle (Fig. 3-102)

The figure at the top left of Fig. 3-102 shows the original picture with one-field component consisting of the effective screen section (within broken lines) and non-effective screen section of the retrace line period. The vertical axis shows the number of horizontal scanning lines (H) and the horizontal axis shows the number (C: Column) obtained by dividing the horizontal scanning period by the 2/3 fsc clock pulse (two-thirds the color subcarrier frequency: luma (Y) signal write sampling frequency) to explain the principles of sub-screen video processing.
The sampling area of the original picture required to compose the sub-screen is shown by the solid lines in the diagram.

Vertical axis : 36H to 228H
Horizontal axis : 31C to 143C

The upper and lower areas outside the effective screen (between 14.5H and 36H and between 228H and 259H) are not sampled due to limitations of memory.
The sampled signal is A/D (Analog/Digital) converted (the amplitude of 1V is quantized to 6 bits for tone) and are then stored temporarily in a DRAM (Dynamic Random Access Memory: called the P in P memory hereafter) for the composition of the sub-screen and time axis conversion. The time axis is reduced by 1/3 sampling and a sub-screen consisting of 64H vertical x 37C horizontal is composed in the P in P memory.
The P in P memory uses an IC which incorporates 4 pairs of memory cell arrays with the memory capacities of 65,536 bits (256 rows x 256 columns) and allocates 6-bit quantized signals to each address by rearranging them to 4 bits. In each pair of memory cell arrays, 256 vertical addresses are divided by four to ensure a sub-screen writing area of 4 field components (64 vertical x 256 horizontal x 4 fields).
Since the sub-screen data must be written to the memory in real time, and simultaneously, the previously written sub-screen data must be read out, the 4 pairs of memory cell arrays are driven in parallel so the write and read modes are the same among these 4. A line memory buffer of 1 row x 256 columns exclusively used for read-out is provided. Writing to the memory cell array is performed at the speed of fsc, the data transfer from the memory cell array to the line memory buffer is at fH and the reading from the line memory buffer is at 4.5 fsc. In previous models, the same two memories were used, however, in this model, one memory is omitted because 6 bits are rearranged to 4 bits and the sampling area for sub picture is reduced. See Item 3-3-6 for details.
With the digital sub-screen data stored in the P in P memory, the field picture data matching the interlace scanning of the main screen is selected and synchronized with the scanning of the main screen and is then read out at the speed of 4.5 fsc. The data is D/A converted and finally replaces the video signal at one of the 4 corners of the main screen. The 62H x 33C area of the sub-screen data consisting of 64H x 37C is displayed on the main screen and the other scanning lines and columns are used for the following 2 purposes.

° Some of the scanning lines and columns are overlapped over the main screen section so the video signal is not missing when scanning is switched from the main screen to the sub-screen and vice versa.

° The other scanning lines/columns align the pedestal levels of the demodulated color-difference signals to match the tints of both the main and sub-screens.

The sub-screen is edged in white to emphasize the border between the sub-screen and main screen. The edge line is determined at 1/fH vertical x 4/4.5 fsc horizontal. During edging, a DC voltage equivalent to 100% white level is superimposed on the video signal for the edge portions. The position of the edge sub-screen framed in the main screen can be selected by the remote control unit to one of the 4 corners of the effective screen as shown at the top right of the figure.
The above is an overview of sampling of the sub-screen and framing it in the main screen. The following describes the actual processing of the video signal for the sub-screen.

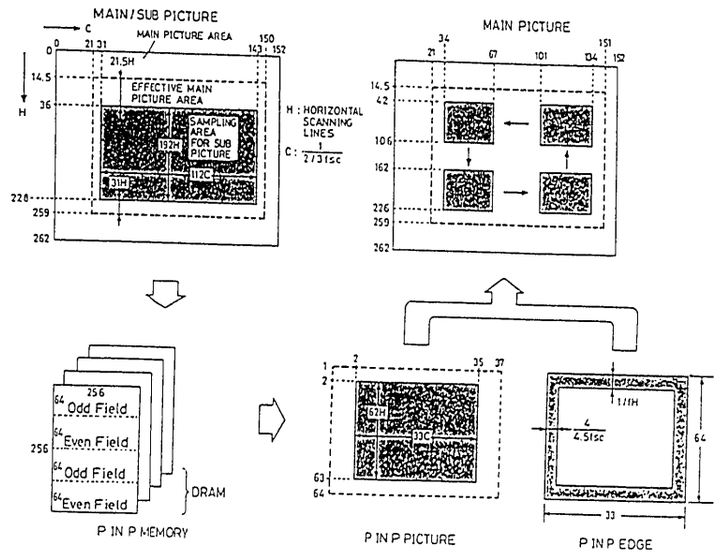


Fig. 3-102 P IN P Picture Developement

3-12-2 P in P video signal processing principle (Fig. 3-103)

The sub-screen specifications are the same as those in the previous model and are summarized in Table 3-102.
The memory capacity (M) required for displaying the sub-screen is as shown by the following equation.

$$M=(fY+f(R-Y)+f(B-Y))\cdot T\cdot m\cdot V\cdot F\cdot n \quad \ldots\ldots \quad (1)$$

fY: Sampling frequency when writing Y
f(R-Y): Sampling frequency when writing R-Y
f(B-Y): Sampling frequency when writing B-Y
T: Display time in horizontal direction (before reduction)
m: Reduction ratio
V: The display lines in vertical direction (before reduction)
F: No. of memory fields
n: Quantized bits

Table 3-102 Sub-screen Specifications

		Y	R-Y	B-Y
Quantized bits (n)		6	6	6
Bandwidth (MHz)		3	0.5	0.5
Sampling frequency	Write	2/3 fsc (2.4 MHz)	1/6 fsc (0.6 MHz)	1/6 fsc (0.6 MHz)
	Read	2 fsc (7.2 MHz)	1/2 fsc (1.8 MHz)	1/2 fsc (1.8 MHz)
Reduction ratio (m)		1/3		
Display position (T x V)		40 µsec x 192H (after reduction: 13.3 µsec x 64H)		
Stored fields (F)		4		

The no. of memory fields (F) is 4, as in the previous model. This is because the control circuit is comparatively simple and the interlacing relation of the sub-screen can always be maintained. When the other values shown in Table 3-102 are entered, the following equation is established.

$$M = (\underset{fy}{2.4\times10^{6}} + \underset{f(R-Y)}{0.6\times10^{6}} + \underset{f(B-Y)}{0.6\times10^{6}}) \times \underset{T}{40\times10^{-6}} \times \underset{m}{\frac{1}{3}} \times \underset{V}{192} \times \underset{F}{4} \times \underset{n}{6}$$

$$= 221{,}184 \text{ (bits)} \quad 256\text{K (bits)}$$

Therefore, one RAM of 256 kbits can satisfy the memory capacity. A dual-port dynamic RAM consisting of 64K words x 4 bits is used for the memory (as in the previous model), however, only one chip is used as 6-bit data is converted to 4 bits for writing and reading. (Since 2 ICs are used for 8 bits in the previous model, the 6-bit data could be processed without being converted.) Because of the above, the frequency for writing and reading must be 6/4 that with current 6-bit processing. In previous model, the Y, R-Y and B-Y data is time shared and sampled (dot sequential method). Assuming that the frequencies for writing and reading are fWD and fRD, the following equation is established using the values shown in Table 3-102.

$$fWD = \underset{Y}{\frac{2}{3}\,fsc} + \underset{R-Y}{\frac{1}{6}\,fsc} + \underset{B-Y}{\frac{1}{6}\,fsc}$$

$$= fsc \text{ (period: 280 nsec)}$$

$$fRD = \underset{Y}{2\,fsc} = \underset{R-Y}{\frac{1}{2}\,fsc} + \underset{B-Y}{\frac{1}{2}\,fsc}$$

$$= 3\,fsc \text{ (period: 93 nsec)}$$

Assuming that the writing and reading frequencies are fW4-bit and fR4 when the 4-bit processing is executed using the dot sequential system,

fW4 = 6/4 fWD = 1.5 fsc (period: 186nsec)
fR4 = 6/4 fRD = 4.5 fsc (period: 62nsec)

Though reading can be performed at 4.5 fsc because of high-speed reading from the serial ports, writing cannot be performed at 1.5 fsc because it is performed from random ports. Therefore, in this model a line sequential system is used so that the luminance and color-difference signals are sampled from different lines.
To reduce the original picture to 1/9, the ratio between the sampling time and read time of the horizontal axis is made 1/3 and the sampling line number of the vertical axis is made 1/3 the total number of scanning lines to compose the sub-screen. If the video signal was processed without being modified, the correct phase information of the burst and chroma signals could not be obtained and the correct tint could not be determined. To prevent this, the video signal of the original picture is separated into the luma signal (Y) and color-difference signals (R-Y, B-Y) and the separated signals are sampled.
The sampling frequencies are approx. 2.4MHz (fsc x 4/6) and 0.6MHz (fsc/6) for the Y signal and R-Y/B-Y signals. Since the maximum frequencies of each signal must be half the sampling frequencies, the frequency bands of the separated and demodulated Y signal are limited by the lowpass filter. The band-limited Y and R-Y/B-Y signals are time-divided by the multiplexer and are applied to the A/D converter.
Since the sampling frequency of the color-difference signals is enough to be approx. 1/4 the frequency of the Y signal and memory capacity must be saved, the multiplexer operates as follows. To sample the Y signal once per three horizontal scanning lines, the Y signal is selected by time-sharing with the rate of 4/6 fsc. Next, to sample the chroma signals from the following first scanning, the B-Y and R-Y signals are selected by time-sharing with the rate of 1/6 fsc alternately.
The A/D converter converts the multiplexer output to a 6-bit digital signal and supplies it to the P IN P Controller to write it to the P in P memory. The P IN P Controller rearranges the 6-bit signal as a 4-bit signal in the processing prior to writing. This signal is supplied to the P in P memory.
When the sub-screen insertion position is reached, the digital Y, R-Y and B-Y signals read from the P in P memory are processed in the reverse way to writing through the demultiplexer, D/A converter and, LPF, and a video signal for the sub-screen whose size is converted is formed. Since the sub-screen is framed correctly at the specified position of the main screen and the same tint must be obtained when the EE video signal is selected for both the main and sub-screens, the sync signal and burst signal in the main-screen video signal are used to time reading from the P in P memory and produce a chroma subcarrier signal necessary for NTSC modulation.

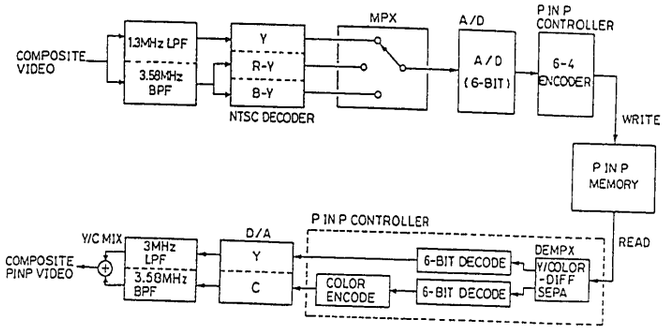


Fig. 3-103 P IN P Video Signal Developement

3-13. Circuit Configuration (Fig. 3-104)
The P in P circuit is between the video output circuit and luma/chroma circuit, the same as the OSD circuit in a VTR with an OSD (On-Screen Display) function. The P in P circuit is on the digital video processing circuit board. Since the digital video processing circuit board handles pulse signals with a maximum frequency of 16MHz (4.5 fsc), it is housed in a shielded case so it does not interfere with other circuits.

The P in P circuit block consists of the following circuits.

1. P in P controller (IC1017)
This receives the two control signals (P in P, P in P POSITION) from the digital control μP and controls the overall P in P circuit as follows.
(1) Sets the VTR to the P in P mode.
(2) Selects the video signals of the main and sub-screens in the P in P mode (P in P Sw/Edge Sw).
(3) Determines the position into which the sub-screen is to be framed.
(4) Generates a multiplexer control signal (MPX Sw).
(5) Determines the clamp timing of the color-difference signals (CLAMP A/D).
(6) Outputs a clock signal for A/D conversion of the sub-screen (AD CLK).
(7) Determines the operation period of the NTSC demodulator (BLP).
(8) Inputs the sync signals separated from the video signals of both the main and sub-screens and judges even/odd field, generates control signals for writing and reading to/from the P in P memory.
(9) Converts the digital sub-screen data read from the P in P memory in parallel to the luminance signal (Y) and color-difference signals (R-Y, B-Y) using the internal demultiplexer and supplies them to the D/A converter after Digital encoding.

2. P in P memory (IC1022)
This IC has the memory capacity of 262,144 bits and stores 4 field picture components of the 6-bit-quantized digital sub-screen video signal rearranged to 4 bits. The writing and reading of data are apparently performed in real time.

3. A/D converter (IC1007)
Converts the sub-screen video signal with the maximum amplitude of 1V separated into the Y, R-Y and B-Y signals to a digital signal quantized to 6 bits. The clock signal necessary for A/D conversion is obtained from the P in P controller.

4. Y signal D/A converter (IC1006)
The D/A converter converts the 6-bit-quantized digital Y signal to an analog signal and then the externally attached lowpass filter (LPF) shapes the waveform and limits it within the specified NTSC bandwidth.

5. P in P reference clock generator (IC1008)
Generates the reference clock (4 fsc) for the P in P controller. The 4 fsc VCO compares the phases of the 1/4 signal of 4 fsc generated here and fsc in the video signal and generates a 4 fsc signal locked to the phase of the chroma subcarrier in the video signal.

6. NTSC demodulator (IC1005)
The NTSC demodulator separates the sub-screen video signal into its luminance and color-difference components to demodulate them; before the demodulator, the externally attached lowpass filter (LPF) and Bandpass filter (BPF) limit the maximum frequency of the signal to be processed to half the sampling frequency.

7. Clamper/Multiplexer (IC1009)
The clamper sets the amplitudes of the R-Y and B-Y signals within the maximum amplitude of the Y signal before A/D conversion and then the multiplexer converts them to serial signals. The Y signals on the (3n + 1) H scanning lines

are time divided by 2/3 fsc. The color-difference signals, (R-Y) and (B-Y) on the (3n + 2) H scanning lines are alternately time divided by 1/3 fsc. The clamp timing signal of the clamper and the time division control signal of the multiplexer are output from the P in P controller.

8. Clock signal generator (IC1014)
Generates clock signals synchronized with the video signals of the main and sub-screens necessary for writing and reading to/from the P in P memory.
  Writing frequency: 14.3MHz (4 fsc)
  Reading frequency: 16.1MHz (4.5fsc)

9. Color-difference signal D/A converter (IC1008)
The D/A converter converts the 6-bit-quantized digital color-difference signals (R-Y, B-Y) to analog signals and the externally attached LPFs limit the chroma signals within the specified NTSC bandwidth.

10. Main/sub video input switch (IC1002)
Selects the video signal supplied to the main and sub-screen video processing circuits. This select command is output from the system control µP.

11. Main-screen sync signal separator circuit (IC1004)
Separates the horizontal and vertical sync signals from the video signals composing the main screen and supplies them to the P in P controller. Receiving both sync signals, the P in P controller determines the display position of the sub-screen and the timing of writing and reading to/from the P in P memory.

12. Sub-screen sync signal separator circuit (IC1005)
Separates the horizontal and vertical sync signals from the video signals composing the sub-screen and supplies them to the P in P controller. Receiving both sync signals, the P in P controller times the reading of the sub-screen signal and determines the display position of the picture in the sub-screen.

13. P in P switch/P in P edge switch (IC1002)
The P in P SW performs switching to frame the sub-screen in the main screen. Then the P in P EDGE SW replaces the edges of the sub-screen video signal with edge signals generated by edge generator. The edge sw output is applied to the RF converter and video output jack.

14. P in P edge generator (IC1002)
Generates a DC voltage equivalent to 100% white level to provide the border between the main screen and sub-screen and applies it to the P in P edge switch.

15. Video input select circuit (IC301, IC303)
The four switches select the video signals from the tuner and line input jack to allow the line and tuner inputs to appear on the main and sub-screens.

16. Digital µP (IC1003)
Receives the operation command from system µP and supplies the P in P and P in P position signals to the P in P controller.

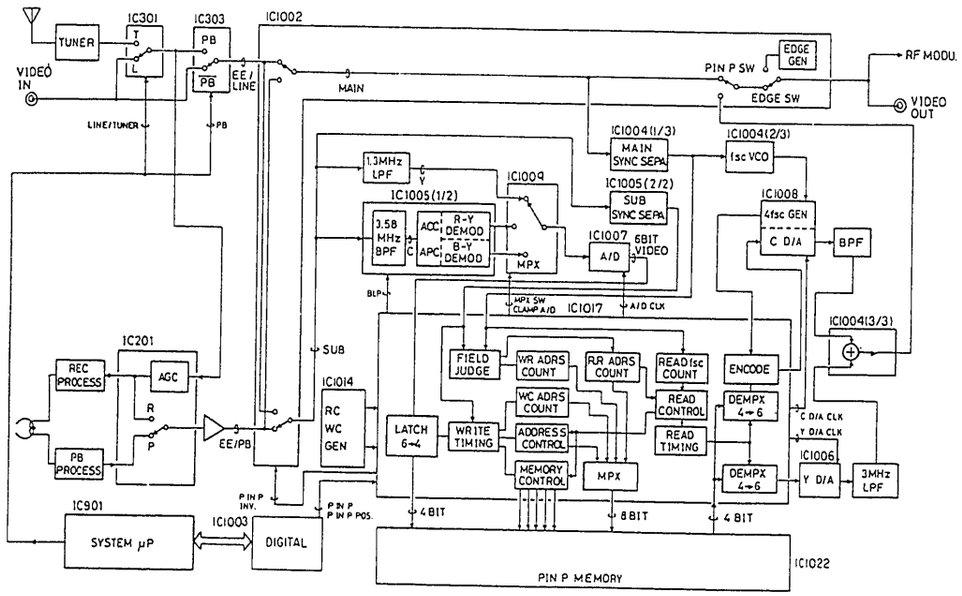


Fig. 3-104 P IN P Block Diagram

3-14. Circuit Operations

The following describes the operations of the individual circuits. The signal processing is explained in the order from the signal input apart except the P in P controller.

3-14-1 P in P controller (Figs. 3-105 to 3-107)

Fig. 2-5 shows the P in P controller, the connections between this and the system control µP (abbreviated to the S-µP hereafter) which controls the controller through the digital µP and the allocation of functions to each pin of the P in P controller.
The P in P controller is connected to S-µP through the digital µP via two control signal lines (P in P POSITION, P in P).
The pictures on the main and sub-screens are swapped by the "P in P INV" signal input to IC1002 (main/sub input switch).
The P in P shift button transmits a signal command to shift the position in which the sub-screen is framed counterclockwise from one of the four corners of the main screen to the next. This key input causes pin 64 "P in P POSITION" of S-µP to generate a single-shot pulse (width 2.25±0.75ms).
Receiving the above three control signals, the P in P controller controls the whole P in P circuit. The detailed operation of each circuit is described later for each item.

To generate these control signals, S-µP receives one key input (P in P/INV. button) from the keyboard of the VTR and two key inputs (P in P/INV. and P in P SHIFT buttons) from the remote control keyboard through the timer µP.
The P in P button sets/resets the P in P mode and inverts the video signals of the main and sub-screens. This key input determines the outputs at pins 62 of S-µP and 42 of D-µP. Pin 41 of D-µP "P in P INV." is a control output to invert the video signals of the main and sub-screens. The output level is:

- "Hi" when the P in P button is pressed again in the P in P EE modes for main/sub-screen conversion.
- Not changed when the P in P button is operated in the P in P EE modes because the main and sub-screens provide the same picture.
- "Hi" when the playback output is selected for the sub-screen in the P in P playback mode and "Lo" in other modes (tuner or line input.)

Pin 42 of D-µP "P in P" outputs a control signal to set the P in P controller to the P in P mode. The output level is "Hi" in the P in P mode and "Lo" in other modes.
The above two outputs are determined as the levels shown in Fig. 2-6 every time the P in P/INV. button is pressed.
The above is summarized in Table 3-103.

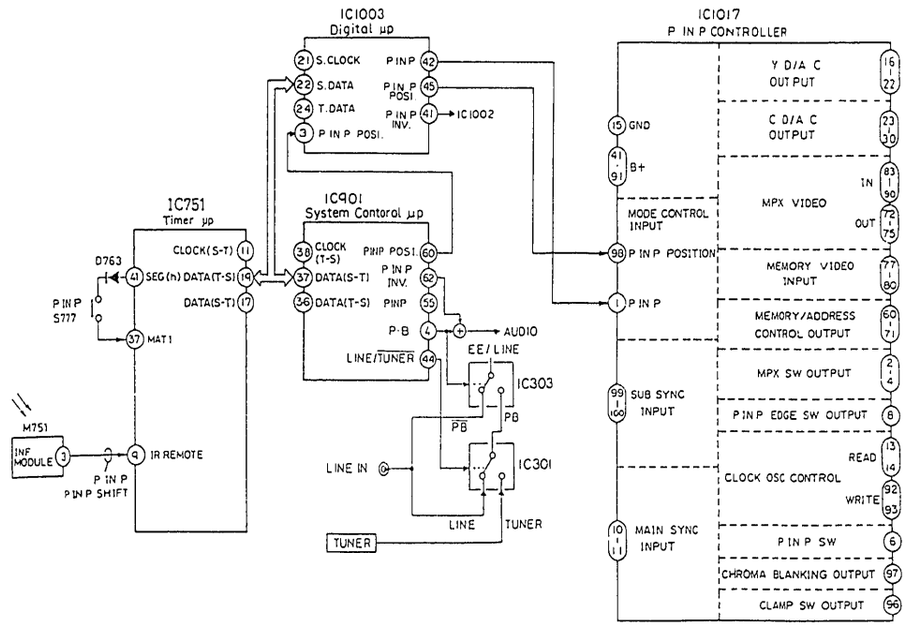


Fig. 3-105 P IN P Controller Circuit

° Field judgement circuit (Fig. 3-108)
The field judgement circuit which is necessary to maintain the interlacing relation of the sub-screen counts the horizontal sync pulses within the vertical sync period in the current model. In this system, both the phases at the rise and fall of the vertical sync signal must be controlled and it is difficult to set the constant of the sync separator. In this model, the field is judged only at the fall of the vertical sync signal.
Fig. 3-108 shows the field judgement circuit diagram and its operation principle in the new system. Flipflop F1 judges whether the rise of the vertical sync signal is present or not within 1/2H from the rise of the horizontal signal. Therefore, the F1 output is considered as a field judgement result basically, but a circuit which prevents malfunctions caused by noise is provided in the later stage.

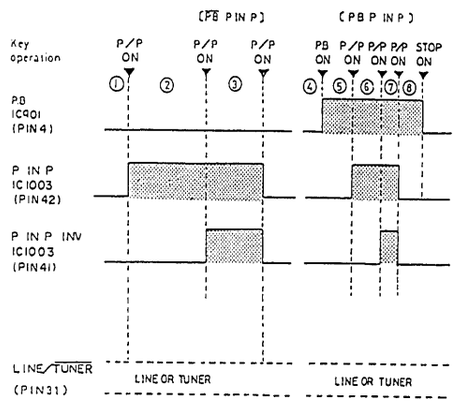


Fig. 3-106 P IN P Control Output Timing Chart

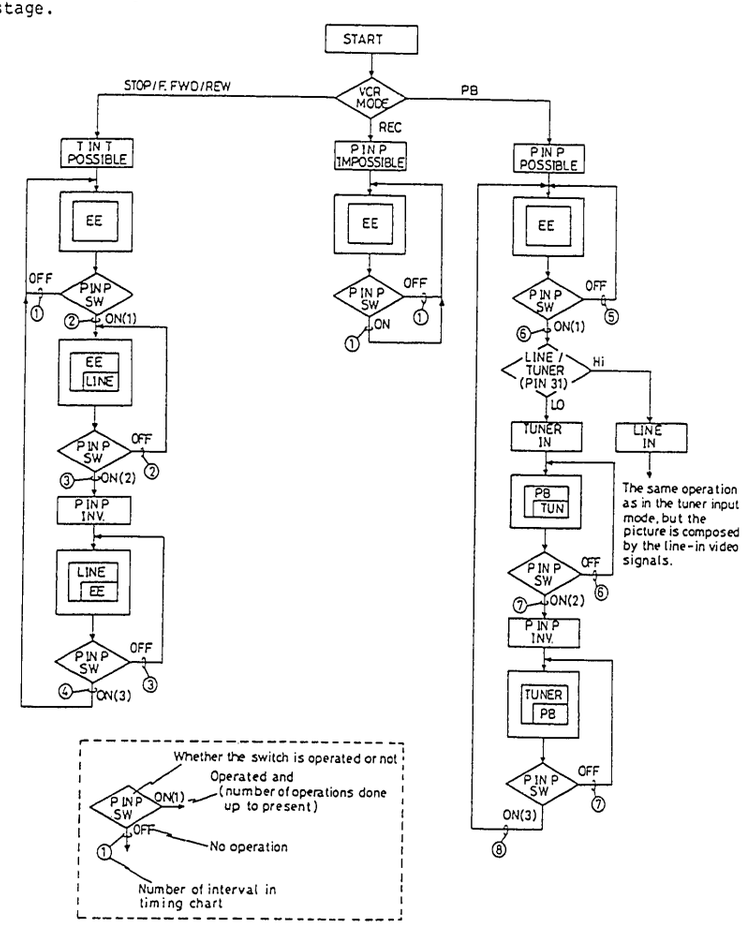


Fig. 3-107 P IN P Operating Flowchart

Table 3-103 Control pins related to the P in P control of D-μP and S-μP

Pin No. D-μP	Pin No. S-μP	I/O	Active Level	Abbreviation	Function
41	62	O	Hi	P in P REV.	Controls the swapping of the main and sub-screens in the P in P mode.
42	61	O	Hi	P in P	P in P mode control output. "Hi" in the P in P mode. (Not used. The P in P output of Digital μP is used)
40	60	O		P in P POSITION	Sub-screen position shift control output. Outputs a pulse every time the SHIFT button is pressed to shift the sub-screen position counterclockwise.

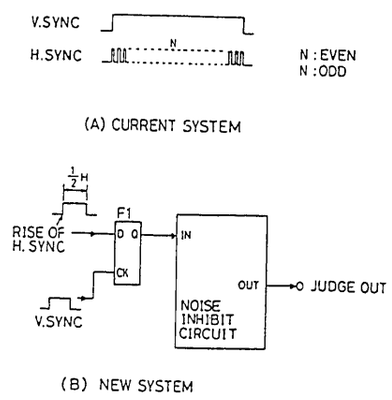
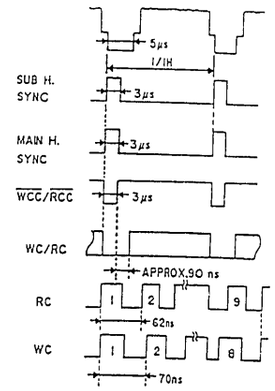


Fig. 3-108 Field Judgement Circuit

3-14-2 Clock signal generator (Fig. 3-109)
The P in P controller provides two-phase clock signals (WC: Write Clock, RC: Read Clock) to process the writing and reading of the sub-screen asynchronously in real time. The WC and RC signals are generated by CR oscillation circuit IC1009 and are supplied to pins 92 and 14 of the P in P controller.

° The WC signal at pin 92 is a clock signal to generate the control signals necessary to write sub-screen data to the P in P memory.
° The RC signal at pin 14 is a clock signal to generate the control signals to read the sub-screen data from the P in P memory, in synchronization with the scanning of the main screen.

To synchronize the oscillation periods of these clock signals with the scanning of the main and sub-screens, the P in P controller supplies two oscillation signals (WCC: Write Clock Clear, RCC: Read Clock Clear) at pins 93 and 13 to IC1014.



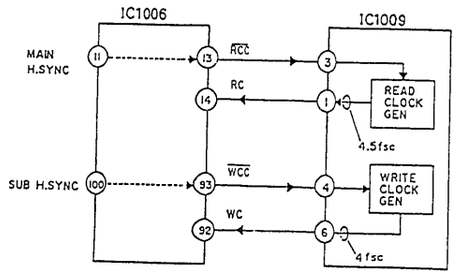


Fig. 3-109 Clock Signal Generator Circuit

Table 3-104 Monitor Output Mode

VCR Mode	Line/TUNER	P in P	P in P Inversion
STOP F.FWD, REW	TUNER	TUNER/LINE	LINE/TUNER
	LINE	LINE/LINE	LINE/LINE
PLAY	LINE OR TUNER	P.B/EE	EE/P.B

° The $\overline{WCC}$ signal at pin 93 and $\overline{RCC}$ signal at pin 13 are negative pulses with a width of 3 µs synchronized with the horizontal signals separated from the sub and main screen video signals respectively. IC1014 stops the oscillations of the RC and WC signals when the $\overline{WCC}$ or $\overline{RCC}$ signal is "Lo".

62 nsec : 70 nsec = 4.5 fsc : 4.0 fsc = RC : WC

3-14-3 Main/sub video input switch (Fig. 3-110)

The video signals supplied to the main/sub video processing circuit in the and P in P mode are selected by IC301 and IC303.
These two ICs provide the pictures shown in Fig. 3-101 in the P in P mode; this is summarized in Table 3-104
IC301 selects the video signal from the built-in tuner or the line input. The control signal is "LINE/$\overline{TUNER}$ ("Hi" when an external input is selected) obtained from S-µP.
IC303 selects the output of IC303 or the line input.

° Selects the output of IC301 in the playback mode because IC901 output pin 4 is "Hi".
° Selects the line input in the $\overline{PB}$ mode.

The video signals supplied to the main and sub video processing circuits are changed over by video input switch IC1002. IC1002 inputs the video signal from the luma/chroma circuit at pin 16 and the video signal from the built-in tuner or video input jack at pin 14 respectively. Then IC1002 selects the video signals output to pins 18 and 2 using the switch control inputs at pins 17 and 19.

° The video signal at pin 18 is selected by the gate circuit controlled by pins 17 and 19 and is supplied to the sub-video processing circuit.
° The video signal at pin 2 is selected by the same gate circuit and is supplied to the main video processing circuit.
° The switch control signal at pin 17 is directly supplied from IC1003 pin 41 (P in P INV) and pin 19 is supplied from pin 42 of D-µP.

As a result, the video signals flowing to the main/sub video processing circuits are as follows.

° STOP/F.FWD/REW Mode
When the Line/tuner sw selects the Line signal, both the main and sub picture consists of the Line signal. When the Line/tuner sw selects the tuner signal, the main/sub picture consists of TUNER/LINE in P in P mode and LINE/TUNER in P in P inversion mode.
° In the playback P in P mode, the main picture consists of the played back signals and the sub picture consists of the tuner or line-in signals.
° In the playback P in P inversion mode (with the P in P button pressed in the P in P mode), the main picture consists of the tuner or line-in signals and the sub picture consists of the played back signals.

IC1002 supplies the output at pin 2 to the main sync separator circuit and the output at pin 18 to the sub-video processing circuit. The main video signal is supplied to the output switch circuit (in IC1002) and main sync

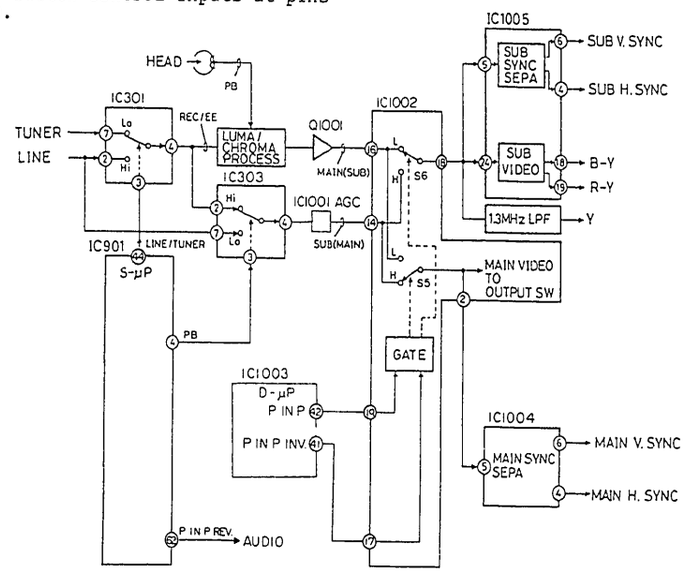


Fig. 3-110 Main&Sub Video Input Switch Circuit

separator circuit (MAIN SYNC SEPA) from pin 2. The sub video signal is supplied to the sub video processing circuit (SUB VIDEO) and sub sync separator circuit (SUB SYNC SEPA).
Table 3-105 shows the button operations to exchange the picture mode.

Table 3-105 MODE TRANSFER CHART

CURRENT PICTURE \ DESIRED PICTURE	EE	EE/EE	EE / PB	EE / STILL	EE/ SLOW SRCH	PB	STILL	SLOW SRCH	PB / EE
EE		P IN P	–	–	–	PLAY	–	–	–
EE/EE	P IN P		–	–	–	–	–	–	PLAY
EE / PB	STOP	–		PAUSE	SLOW SRCH	P IN P	–	–	–
EE / STILL	–	–	PAUSE		–	–	–	–	–
EE / SLOW SRCH	STOP	–	PLAY	–		–	–	–	–
PB	STOP	–	–	–	–		PAUSE	SLOW SRCH	P IN P
STILL	STOP REC	–	–	–	–	PAUSE		SLOW SRCH	–
SLOW SRCH	STOP	–	–	–	–	PLAY	–		–
PB / EE	STOP	–	P IN P	–	–	–	PAUSE	SLOW SRCH	

NOTE : "/ " MEANS "MAIN/SUB PICTURE "

3-14-4 Sync signal separator (Fig. 3-111)

The sync signals necessary for the write/read control of the P in P memory are separated from the SUB VIDEO signal and the MAIN VIDEO signal. The sync signal separated from the MAIN VIDEO signal is called the "MAIN SYNC" and the sync signal separated from the SUB VIDEO signal is called the "SUB SYNC". SUB SYNC is utilized during the writ mode. On the other hand, MAIN SYNC is utilized durinrg the read mode.
The SUB SYNC signal is separated by the sub-sync separator (SUB SYNC SEPA) circuit (IC1005) from the sub-screen signal and the MAIN SYNC signal is separated by the main sync separator (MAIN SYNC SEPA) circuit (IC1004) from the main video signal. IC1004 separates the composite sync signal (C. SYNC) from the MAIN VIDEO signal input via pin 5 using the sync separator (SYNC SEPA.) and supplies its output to the AFC circuit and BGP generator. The AFC circuit together with the voltage-controlled oscillator (32 fH VCO) synchronizes the 32 fH VCO oscillation frequency with the horizontal sync signal separated from the composite sync signal. Through this sync operation, a horizontal sync signal (MAIN H SYNC) without an equalizing pulse or external noise is obtained. To synchronize the output obtained by dividing the 32 fH VCO oscillation output by 32 with the horizontal sync signal separated from the composite sync signal, the AFC circuit detects the frequency error voltage between these signals and feeds it back to the 32 fH VCO to correct its oscillation frequency.
The MAIN H SYNC signal is supplied to pin 11 of the P in P controller.

The composite sync signal obtained at pin 9 of IC1004 passes through the LPF consisting C1114 and comparator Q1007 and reenters IC1004, and the H. SYNC components are removed and only the V. SYNC signal is extracted by the vertical sync separator. The LPF and comparator between pins 9 and 7 are newly added when compared to the previous model. These components integrate and shape the sync signal previously before the V. sync separator in IC1004 so that the V. sync separation is possible even with a prerecorded tape on which the vertical equalizing pulse is wider (tape with copyguard). The V. SYNC signal is supplied to pin 10 of the P in P controller.
The SUB SYNC signal is sync separated by IC1005. The SUB H. SYNC signal is processed in the same way as the MAIN H. SYNC and is supplied to pin 100 of IC1017. The SUB V. SYNC signal is processed in the approximately same way as the MAIN V SYNC and is supplied to pin 99 of IC1017. The only difference is that the TRICKPLAY signal is applied via DT1001 to the reference voltage generator connected to the positive terminal of the comparator Q1008. This raises the threshold level of the comparator and prevents jitter which tends to occur during trickplay because noise is applied

to the sync signal.
The P in P controller inputs above sync signals and judges whether it is an odd or even field, and generates the P in P Memory Control signals necessary to write and read the sub-screen data simultaneously to/from the P in P memory. See the "P in P memory" for details.

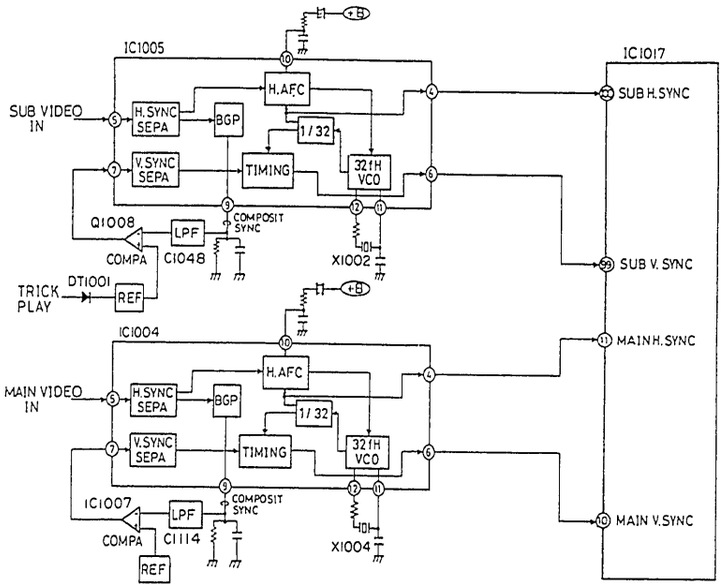


Fig. 3-111 SYNC SEPA. Circuit

3-14-5 NTSC demodulator, MPX, A/D converter (Fig. 3-112)

Fig.3-112 shows the process circuit in which the sub-screen video signal selected by the main/sub video input switch is converted to a digital signal up to its input to the P in P controller. This circuit consists of the following.

- NTSC demodulator (IC1005) which demodulates the video signal into luminance and color-difference signals.
- Multiplexer (IC1009) which clamps the luminance and color-difference signals within the sampling range of the A/D converter and converts them to serial signals.
- A/D converter (IC1007) which converts the luminance and color-difference signals, converted to serial signals, to a digital signal quantized to 6 bits.
- The P in P controller (IC1017) which controls these three ICs.

(A) IC1005 receives the sub-screen video signal (SUB VIDEO) at pins 5 and 24 and operates the following.

1. Generates the burst gate pulse (BGP) necessary to demodulate the color-difference signals.
2. Separates the luminance signal and then limits the bandwidth to less than half the sampling frequency (CP1001: 1.3 MHz LPF).
3. Limits the bandwidth of the R-Y and B-Y color-difference signals by the 3.58MHz BPF before demodulating them. (Pin 24, CP1004).

(BGP generation)

To determine the phase of the BGP signal, IC1005 separates the horizontal sync signal from the sub video signal input to pin 5 from the H. SYNC separator and applies it to the BGP generator. The BGP generator delays the horizontal sync signal by approx. 2.5 µsec and then shapes it to a square wave with a width of approx. 3.5 µsec. (See Fig. 3-113 (A)).

The luminance signal is separated by the 1.3MHz lowpass filter (CP1001) and is limited to less than half the sampling frequency and is then applied to pin 13 of the multiplexer (IC1009).
The color-difference signals, B-Y and R-Y, are demodulated by the same processing as in a TV receiver. The demodulated color-difference signals were previously limited by the external 3.58MHz BPF and are then applied to pins 9 and 11 of IC1009.

IC1005 stops the inputs to the

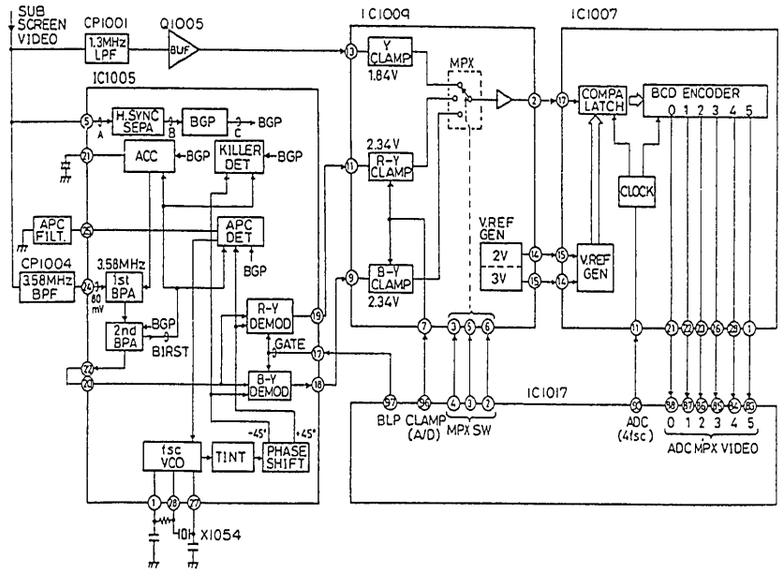


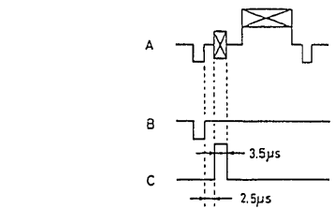
Fig. 3-112 NTSC Demod/MPX/AD Converter Circuit

demodulator circuit (R-Y MOD, B-Y MOD) to reduce noise at the clamp points of the color-difference signals in the horizontal retrace period. This is controlled by the gate (controlled by pin 17) in the demodulator and the P in P controller. The P in P controller generates the control signal (BLP) of the gate using the sync signal separated from the video signal which is selected for the sub-screen and outputs it at pin 97. The phase of the BLP signal is the same as that of the horizontal sync signal and its pulse width is determined to 12 µs, equivalent to the horizontal retrace period (See Fig.3-113(C)). The BLP signal turns off the gates in the demodulator. Therefore, the demodulators (R-Y DEMOD, B-Y DEMOD) in IC1005 output the signal with noise on the pedestal line reduced.

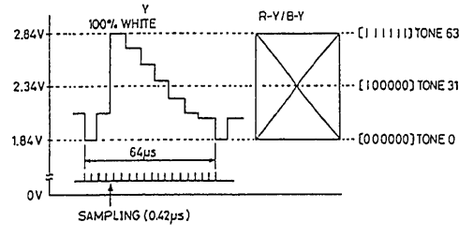
(B) IC1009 inputs the luminance (Y) and color-difference signals (R-Y, B-Y) from CP1001 and IC1005 via pins 13, 9 and 11 respectively and operates the following.

1. Sets the maximum amplitudes of each signal within the sampling range of the A/D converter using the clampers (Y CLAMP, R-Y CLAMP, B-Y CLAMP) corresponding to each signal.
2. Converts each signal to serial using the multiplexer (MPX).

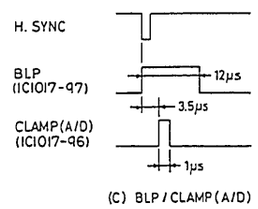
The setting voltages of the Y, R-Y and B-Y CLAMPs are obtained by dividing 5V by three ladder resistors. The sync tip of the luminance signal (Y) is set to 1.84V by Y CLAMP. The voltage of color-difference signals (R-Y, B-Y) corresponding to the sync tip period of the luminance signal is determined to



(A) BGP GEN



(B) CLAMP LEVEL

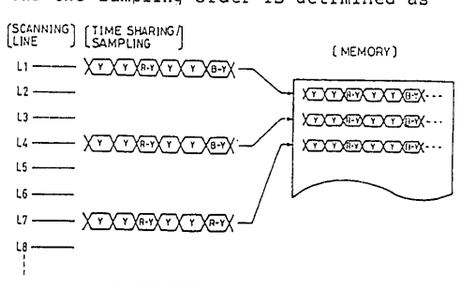


(C) BLP / CLAMP (A/D)

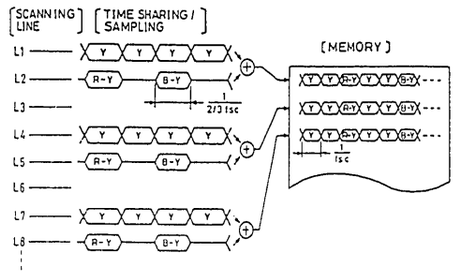
Fig. 3-113 Timing Charts

2.34V, that is 0.5V higher than the luminance sync tip level. Since the maximum amplitude of the Y signal is set to 1V as shown in Fig.3-113 (B), half the voltage (2.34V) of the maximum amplitude of the Y signal becomes the clamp voltage of the R-Y and B-Y signals. The clamp timing of the R-Y and B-Y signals is determined by the P in P controller. The P in P controller generates a clamp control signal (CLAMP (A/D)) using the horizontal sync signal separated from the video signal which was selected for the sub-screen and outputs it at pin 96. The CLAMP (A/D) signal is determined as a pulse with a width of 1 µs which is delayed from the trailing edge of the horizontal sync signal by 3.5 µs. (See Fig.3-113(C)) This signal is supplied to the B-Y and R-Y CLAMPs via pin 7 of IC1009.

The multiplexer (MPX) receives the clamped Y, R-Y and B-Y signals and converts them to serial signals using the 3-phase MPX control signals supplied from the P in P controller. The P in P controller generates the MPX control signals (Y MPX SW, B-Y MPX SW, R-Y MPX SW), synchronized with the horizontal and vertical sync signals separated from the video signal which was selected for the sub-screen, and outputs them at pins 4, 2 and 3. Sampling of the sub-screen is performed at 2/3 fsc for the Y signal and at 1/3 fsc for the color-difference signals (at 1/6 fsc for each R-Y and B-Y) and the sampling order is detrmined as follows.



(A) DOT SEQUENTIAL SYSTEM PRINCIPLES



(B) LINE SEQUENTIAL SYSTEM PRINCIPLES

Fig. 3-114 Dot/Line Sequential Systems

The Y signal is sampled in the (3N + 1) H periods and the color-difference signals are sampled in the (3n + 2) H periods.

1st H: Y → Y → Y ----- Y
2nd H: (B-Y) → (R-Y) → (B-Y) -----(R-Y)
3rd H: not sampled
4th H: Y → Y → Y ----- Y
5th H: (B-Y) → (R-Y) → (B-Y) -----(R-Y)

The above sampling is called the line sequential system, which is different from the dot sequential system used in the previous model. The reason why the line sequential system is employed in the new model is as previously described in 3-12General. Fig.3-114 (A) shows the principle of the dot sequential system. In the dot sequential system, the Y and the color-difference signals (R-Y and B-Y) are sampled from the 1st, 4th, 7th, ... scanning lines by time sharing. Fig.3-114 (B) shows the principle of the line sequential system. In the line sequential system, the Y signal is sampled from the first, 4th, 7th ... scanning lines and the color-difference signals (R-Y and B-Y) are sampled from the 2nd, 5th, 8th ... scanning lines. In the line sequential system, the LUMA/CHROMA displacement of 1/3 line component occurs in the vertical direction of the sub-screen in principle, but there is no actual problem in the sub-screen. Since the color-difference signals tend to be delayed by the comb filter in the vertical direction with latest VTRs and TVs, the line sequential system works to correct the delay. Fig.3-115 shows the MPX operation timing. The Y, R-Y and B-Y signals converted to serial signals are supplied to pin 2 of IC1009.

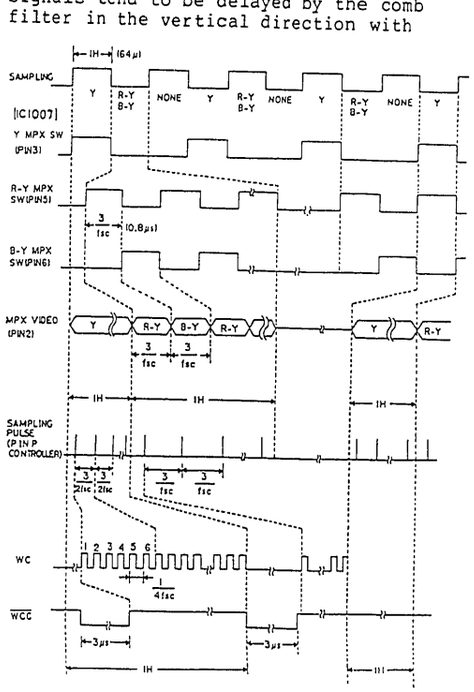


Fig. 3-115 MPX Sampling Timing Chart

(C) IC1007 receives the Y, R-Y and B-Y signals converted to serial signals at pin 17 and converts them to digital signals quantized to 6 bits and then applies them to pins 83 to 88 of the P in P controller.
The reference voltage necessary for A/D conversion is obtained from the reference voltage generator (V REF GEN) at pins 14 and 15 of IC1009 and the clock signal is from pin 90 of the P in P controller.
The V REF GEN generates the maximum and minimum reference voltages for A/D conversion. The minimum voltage is determined as 2V and the maximum as 3V to cope with the maximum input amplitude, 1Vp-p. These two reference voltages are applied to the reference voltage generator (V REF GEN) at pins 15 and 14 of IC1007. This V. REF GEN divides the voltage (1V) obtained by subtracting the minimum voltage (2V) from the maximum voltage (3V) evenly to 1/64 by the ladder resistors and applies the divided voltages to the comparator/latch circuit (COMPA/LATCH).
The COMPA/LATCH compares the MPX output voltage at pin 17 and the 64-step reference voltage applied from the V REF GEN when the clock signal equivalent to 4 fsc which is supplied from pin 90 of the P in P controller is "Hi", and when the clock signal is "Lo", the COMPA/LATCH is set to a mode to latch the comparison result and applies the output to the BCD encoder.
The BCD encoder codes the comparison result of the COMPA LATCH to 6 bits and applies the outputs to pins 83 to 88 of the P in P controller.

3-14-6 P in P memory (Figs. 3-116 to 3-121)

(A) Sampling and memory
(Figs. 3-116 to 3-119)

Figs. 3-116 and 3-117 are simulation diagrams showing the relationship between writing and reading to/from the memory. The figures show one row component of the memory. The actual memory has 256 rows. As described previously, the luminance signal (Y) and color-difference signals (C) (R-Y, B-Y) are sampled from the different lines and the resultant data is written to the memory. The writing frequency is fsc in basic units. The Y signal is written for every sampling and the C signal is written at a frequency of three per six samplings. The row addresses are controlled as 1, 3, 5, 6, 7, 8, 10 ... when writing the Y signal and as 0, 2, 4, 9, 11, 13 ... when writing the C signal.
This is explained as below, following the figures.

(1) The Y signal is sampled at 3/(2 fsc) to be a 6-bit digital signal.
(2) Since the P in P memory consisting of 4 bits, it rearranges this 6-bit digital signal as follows:
First, 4 bits are fetched from 6 bits.
Then the remaining 2 bits are fetched together with 2 bits of the adjacent sampling data and processed as one unit of 4-bit data. Repeating this procedure rearranges 6-bit data as 4-bit data.
(3) This 4-bit data is stored (written) to the column address of the specified memory at 1/fsc cycle.
(4) The column addresses to which the Y signal is written are repeated at a cycle of 9 addresses as follows.

	1		3		5	6	7	8
	10		12		14	15	16	17

(5) The line next to the sampled Y signal is sampled at 1/3 fsc for the color-difference signals. The R-Y and B-Y signals are sampled alternately. 12 bits obtained by a pair of samplings of R-Y and B-Y are rearranged to 4 bits x 3 units.
(6) A pair of R-Y and B-Y sampled at 6/fsc are rearranged to the following 3 units.
° 4 bits of R-Y
° Remaining 2 bits of R-Y and 2 bits of B-Y
° Remaining 4 bits of B-Y
This operation is performed at fsc as a pair and repeated at 6/fsc.
(7) From the data consisting 4-bit x 3-unit, 3-unit data is stored in the blank addresses, corresponding to those in which the Y signal is stored, at 1/fsc. The next 3-unit data is stored repeatedly after 4/fsc.

0		2		4				
9		11		13				

Fig. 3-118 shows the timing of writing to the memory. In the previous model, two 3 fsc (10.7 MHz) signals which are shifted by a half cycle with respect to each other are used as a reference clock to provide the write timing and the delay of half cycle must be adjusted (function trimming in the module). With a new P in P controller, since one 4 fsc reference clock (14.3 MHz) provides the write timing, this adjustment is not required. An early write cycle that writes data at the fall of $\overline{CAS}$ is used for the memory mode. The counter clock signals which generate column addresses during writing are different for the lines to which the Y and C signals are written as shown in

the figure.
In the line sequential system, "sampling of Y signal", "sampling of (R-Y)/(B-Y) signals" and "not sampling" are repeated for each line from the sampling area composing one field (262.5H) of the sub-screen.
The writing cycle of a signal per line (64 µsec) is 1/fsc (280ns) and are repeated about 150 times (230= 64µs/280ns). The operation within 280 nsec (using the write clock (4 fsc) as a reference clock) is as follows.
The reference clock (WC) for data write is 4 fsc.
The clock for the A/D converter (A/D C CLOCK: 4 fsc) is the same as WC.
The $\overline{RAS}$ (ROW ADDRESS STROBE: row address designation clock) is a pulse with the cycle of 1/fsc, "Hi" period of 3/(8 fsc) and "Lo" period of 5/(8 fsc) which designates a row address at its fall. It reads data (row address) from the row counter at each fall to designate a row address.
The $\overline{CAS}$ (COLUMN ADDRESS STROBE: Column address designation clock) is a pulse with the cycle of 1/fsc, the "Hi" period of 5/(8 fsc) and "Lo" period of 3/(8 fsc) which designates a column address at its fall. It reads data (column address) from the column counter at each fall to designate a column address.
The address data consists of row data: 1/(4 fsc) and column data: 3/(4 fsc) repeated and each data is read at the falls of the $\overline{RAS}$ and $\overline{CAS}$ signals as address codes.
The column counter updates the addresses each time a 2 fsc clock is input. The clock number (addresses) of the counter is read at the fall of $\overline{CAS}$ as shown in the timing chart. As can be seen in Fig. 2-16, the clocks of the column counter when writing the color-difference signals are "0", "2", "4", "none", "none", "none", "9" ...
With the sampled color-difference signals,

- 4 bits of R-Y to address 0
- 2 bits of R-Y and 2 bits of B-Y to address 2
- 4 bits of B-Y to address 4

are written consequently at 1/fsc and then writing is stopped for a period of 1/fsc x 4 to complete one cycle (1680 nsec). The clock of the column counter when writing the luminance signal are "1", "3", "5", "6", "7", "8", "10", ...
The Y signal data sampled with 6 bits at 3/(2 fsc) is rearranged to 4-bit data and then written to the above addresses.
Fig.3-119 shows the timing during reading. The 4.5 fsc (16.1 MHz) signal is used as a reference clock and this is utilized as a serial read clock without being modified. The data is read from the memory in sequence from address 0 and the data arrangement reverse to writing is performed; Y signal data is supplied to the D/A converter and the C signal data to the encoder as 6-bit data with the timing shown in the figure.

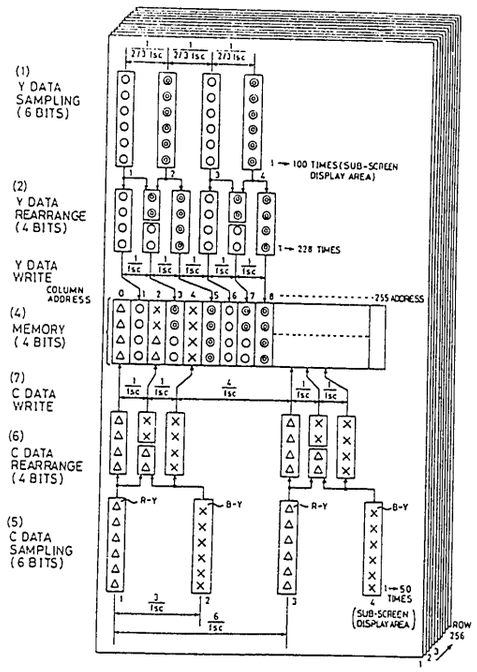

(1) Y DATA SAMPLING (6 BITS)
(2) Y DATA REARRANGE (4 BITS)
Y DATA WRITE COLUMN ADDRESS
(4) MEMORY (4 BITS)
(7) C DATA WRITE
(6) C DATA REARRANGE (4 BITS)
(5) C DATA SAMPLING (6 BITS)
1 — 100 TIMES (SUB-SCREEN DISPLAY AREA)
1 — 228 TIMES
255 ADDRESS
R-Y
B-Y
1 — 50 TIMES (SUB-SCREEN DISPLAY AREA)
ROW 256

Fig. 3-116 Writing to Memory

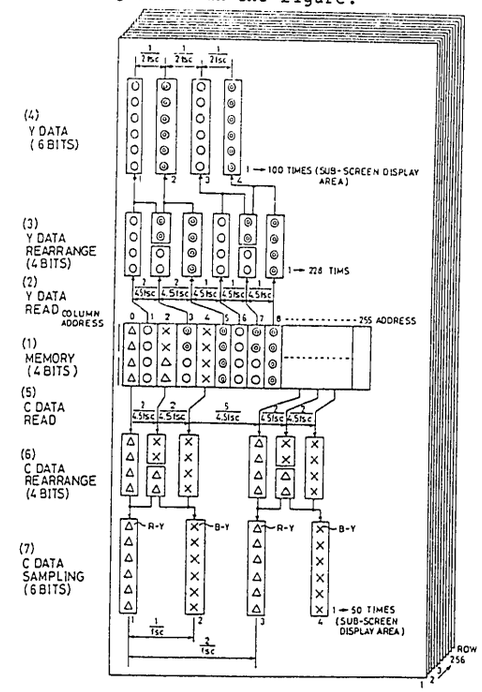

(4) Y DATA (6 BITS)
(3) Y DATA REARRANGE (4 BITS)
(2) Y DATA READ COLUMN ADDRESS
(1) MEMORY (4 BITS)
(5) C DATA READ
(6) C DATA REARRANGE (4 BITS)
(7) C DATA SAMPLING (6 BITS)
1 — 100 TIMES (SUB-SCREEN DISPLAY AREA)
1 — 228 TIMS
255 ADDRESS
R-Y
B-Y
1 — 50 TIMES (SUB-SCREEN DISPLAY AREA)
ROW 256

Fig. 3-117 Reading from Memory

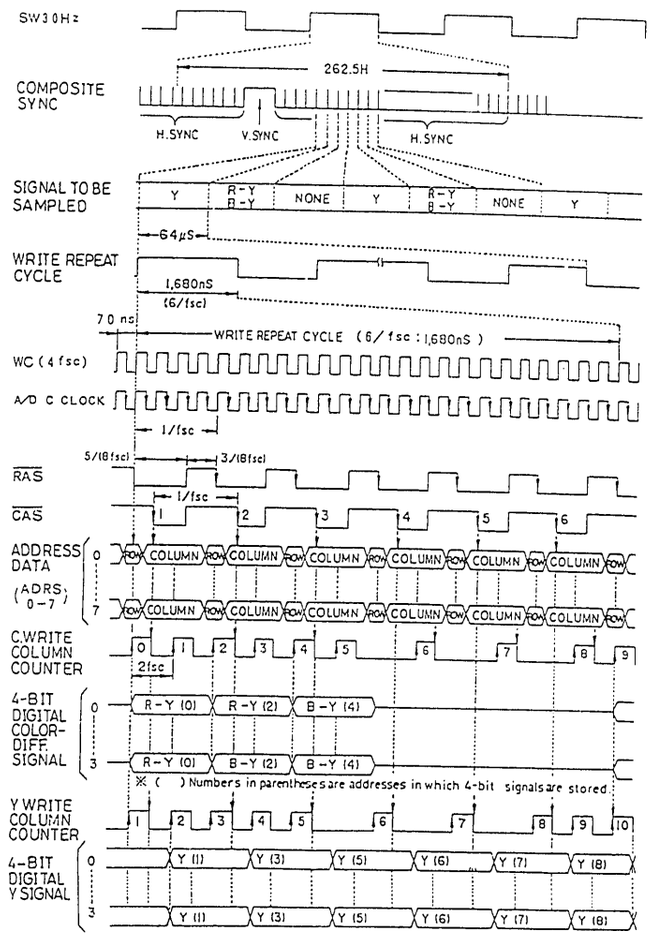


Fig. 3-118 Write Timing Chart

(B) Memory circuit (Figs.3-220 and 3-221)
Fig. 3-220 shows the P in P memory and the P in P controller which controls it. The P in P memory uses one chip on which 4 pairs of memory cell arrays of 256 x 256 bits are provided and 4 pairs are allocated to each bit of the 6-bit digital sub-screen data by rearranging it as 4 bits. Since writing and reading of the digital sub-screen data must be performed the time axis convension asynchronously in real time, the P in P memory has a line buffer memory (LINE BUF MEM) exclusively for reading.
The LINE BUF MEM is in the P in P memory; 1H-component data (256 bits) is transferred from the memory cell array when one address is designated and the transferred data is read by the serial clock exclusively for reading. Using this memory, writing to the memory cell array is performed every time the sub-screen is sampled (at the fsc speed) by designating the address. Data transfer from the memory cell array to the LINE BUFF MEM is performed in every time horizontal scanning of the main screen which started (at the fH speed) by designating the address. Reading from the LINE BUF MEM is performed with the timing of the serial clock signal equivalent to 4.5 fsc without designated addresses. Since one writing routine is completed when it is performed six times at fsc and reading nine times at 4.5 fsc is required, the following equation is established.

$$1/fsc \times 6 : 1/(4.5\ fsc) \times 9 = 3 : 1$$

Therefore, the time axes are shortened to 1/3 and the video signals of the 1/9 size sub-screen are generated. As the asynchronous clock signals are used for both writing and reading, different

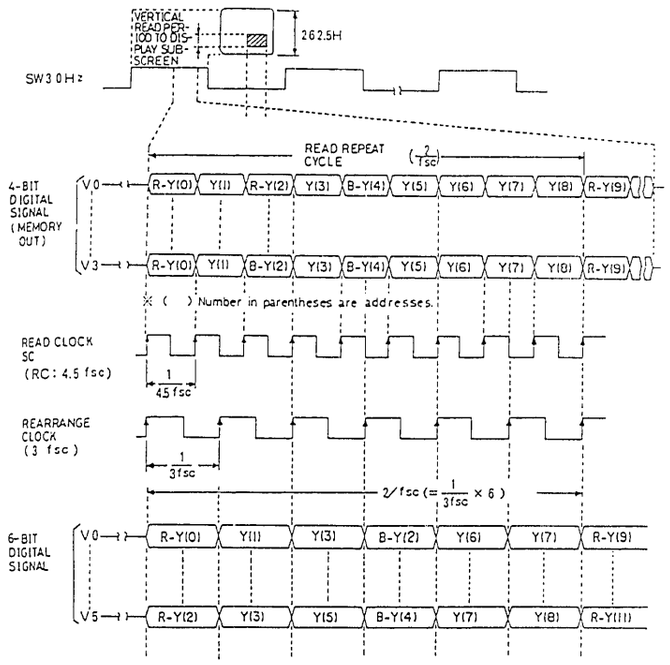

VERTICAL READ PERIOD TO DISPLAY SUB-SCREEN
262.5H
SW 30Hz
READ REPEAT CYCLE
4-BIT DIGITAL SIGNAL (MEMORY OUT)
V0
V3
R-Y(10) Y(1) R-Y(2) Y(3) B-Y(4) Y(5) Y(6) Y(7) Y(8) R-Y(9)
B-Y(2) Y(3) B-Y(4) Y(5) Y(6) Y(7) Y(8) R-Y(9)
※ ( ) Number in parentheses are addresses.
READ CLOCK SC (RC: 4.5 fsc)
1/4.5 fsc
REARRANGE CLOCK (3 fsc)
1/3fsc
2/fsc (= 1/3fsc × 6)
6-BIT DIGITAL SIGNAL
V0
V5
R-Y(0) Y(1) Y(3) B-Y(2) Y(6) Y(7) R-Y(9)
R-Y(2) Y(3) Y(5) B-Y(4) Y(7) Y(8) R-Y(11)

Fig. 3-119 Read Timing Chart

patterns can be selected for the main and sub-screens.
When receiving the signals quantized to 6 bits, the P in P controller samples the Y signal data every 2/3 fsc. Since the color-difference signal data was previously time-shared by the MPX SW output, the controller samples a pair of R-Y and B-Y data in every time-sharing unit. Then the controller rearranges this data as 4 bits.
Since priority is given to reading from the memory cell array to LINE BUFF MEM over writing to the memory cell array, the P in P controller has a temporary standby memory (STACK) for the written data. The STACK consists of 6 bits and each bit is allocated to 6 pairs of memory cell arrays. The STACK is triggered by the horizontal sync signal of the main screen to stack the data to be written to the P in P memory temporarily for the 1/fsc period and outputs it in the next cycle.
Since the sub-screen data with the same field as the odd or even field of the main screen and one field of which has been completely written must be applied to the main screen according to the interlace scanning, the P in P memory has an area in which the sub-screen data of 4 fields can be written for each 4 pairs of memory cell arrays (see Fig. 3-120). One field is incomplete as writing is being done, and the other 3 fields are completely writen. One of these 3 is selected according to the odd/even fields of the main screen and is read.
To detect the even/odd fields of both the main and sub-screens, the P in P controller detects the phase relations of the horizontal/vertical sync signals separated from both the main and sub-screen video signals to determine the odd or even field. The field detection output of the sub-screen determines the address of the field to which the sub-screen is written, and the field detection output of the main screen determines the address of the sub screen that is same field as the main screen and is completely writen.
The sub-screen data read from the LINE BUF MEM in the P in P memory is converted in parallel to three signals, Y, B-Y and R-Y, by the demultiplexer (DEMPX) in the P in P controller shown in Fig. 3-120.
Since the color-difference signals are quadrature 2-phase-modulated (color digital encoder) at this time, the signals output from the P in P controller become NTSC color signals.
A DRAM (Dynamic Random Access Memory), data in which needs rewriting (refreshing) within 4 ms after writing, is employed as the P in P memory. Since refreshing is performed in reading as well in writing, timing is determined so writing or reading to/from each memory cell array is performed within 4 ms in this unit. Therefore, the refreshing operation is not performed on its own.

Since data must be processed at the maximum speed of 4.5 fsc, a 4-bit parallel single-direction bus is used for data writing/reading and an 8-bit parallel single-direction bus is used for address data.
To control the writing of data on three data buses and to determine the operation mode of the P in P memory, the P in P controller supplies the 5-bit control signals ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, SC, $\overline{DT}$) to the P in P memory.
The $\overline{RAS}$ output determines the write timing of the row address data, write mode data and read mode data. The row address data, write mode data and read mode data are prepared on the address bus, $\overline{WE}$ line and $\overline{DT}$ line respectively and are written to the P in P memory when the $\overline{RAS}$ changes from "Hi" to "Lo".
The $\overline{CAS}$ output determines the write timing of the column address data. After the row address data is written to the P in P memory, the column address data is prepared on the address data bus and is written to the P in P memory when the $\overline{CAS}$ changes from "Hi" to "Lo".
The $\overline{WE}$ output controls the write mode of the P in P memory and the write mode of the sub-screen data. The P in P memory has late write and early write modes. In this model the early write mode is used to write digital video signals. The $\overline{WE}$ must be held at "Lo" to set this write mode when the $\overline{CAS}$ changes from "Hi" to "Lo". After the row and column addresses are written to the P in P memory, the sub-screen data on the write data bus is written to the P in P memory when the $\overline{CAS}$ changes from "Hi" to "Lo".
The $\overline{DT}$ output determines the read mode of the P in P memory. There are data transfer and data read modes. In the data transfer mode, the 1 H data in the memory cell array is transferred to the line buffer memory. In the data read mode, the data on the line buffer memory is output from IC1022. When the $\overline{RAS}$ changes from "Hi" to "Lo", the read mode is entered if the $\overline{DT}$ is held at "Hi" and the data transfer mode is entered if the $\overline{DT}$ is held at "Lo". In the read mode, the address data which is designated in the data transfer mode is read at the rise of the serial clock signal (SC) equivalent to 4.5 fsc. The data transfer mode is executed when the $\overline{RAS}$ and $\overline{CAS}$ change from "Lo" to "Hi" after the row and column addresses are designated.
The SC output is a serial clock signal equivalent to 4.5 fsc which is necessary to read data from the line buffer memory when the P in P memory is set to the read mode. The data is read at the rise of the SC.

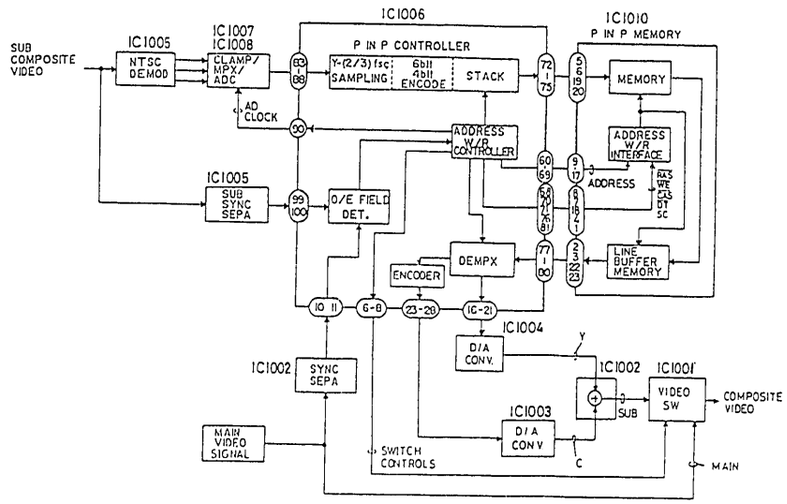


Fig. 3-120 P IN P Memory Circuit

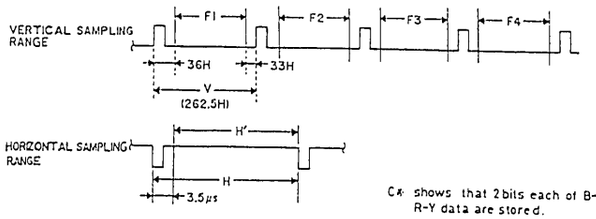


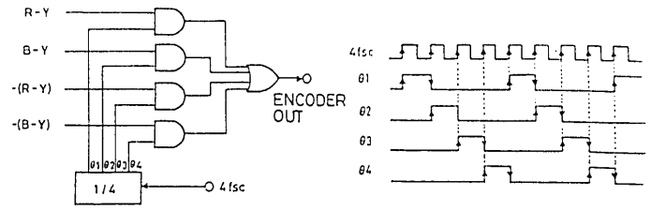
Fig. 3-121 P IN P Memory Map

3-14-7 Digital encoder (Fig.3-122)

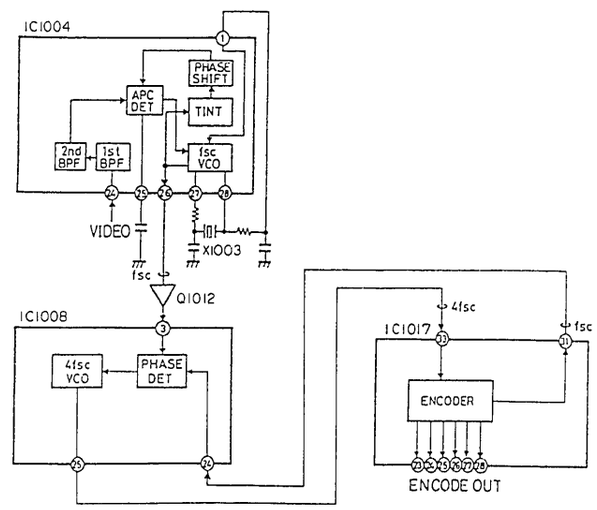
In the previous model, the R-Y and B-Y signals are encoded (quadrature 2-phase modulated) by the encoder module consisting of encoder IC and its peripheral circuits after D/A conversion. In this model, the signals are encoded digitally within the P in P controller to reduce the number of parts.
Fig.3-122 (A) shows the principle of the digital encoder (one bit component). The signals 1 - 4 with a cycle of fsc and with phases different by 90° are produced from 4 fsc whose phase is locked to the subcarrier in the main video signal and four signals, R-Y, B-Y, -(R-Y) and -(B-Y), are selected. When the 6-bit encoder outputs are passed through the D/A converter and 3.58 MHz bandpass filter, the modulated chroma signal whose tint matches that of the main video signal can be obtained.

(A) fsc generation
The fsc signal used for the color-difference signal digital encoder clock generator (IC1008) is produced by the fsc VCO in IC1004 and the APC loop.
The Fsc VCO, combined with the phase comparator (APC), is controlled so that the oscillation frequency, fsc, of the fsc VCO and the burst signal in the main video signal are synchronized. The APC receives the output of the fsc VCO and burst signal extracted by the 2nd BPA and detects the phase error voltage of both signals which is smoothed by capacitor at pin 25. The smoothed phase error voltage is applied to the fsc VCO to correct its oscillation frequency. The fsc VCO oscillates because of the 3.58 MHz crystal oscillator (X1003) connected to pins 27 and 28.

(B) Generation of clock for digital encoder
The chroma subcarrier (fsc) necessary to modulate the D/A converted R-Y and B-Y color-difference signals to chroma signals are produced from the output of 4 fsc VCO in IC1008. The output of 4 fsc VCO (IC1004) and fsc output from pin 31 of the P in P controller are phase compared to drive the 4 fsc VCO, thus obtaining the chroma subcarrier.
The output of 4 fsc VCO is output from pin 25 of IC1008 and is applied to the P in P controller. The digital encoder in the P in P controller divides this 4 fsc by four and produce a clock with its phase shifted by 90° for every 1/4 by a phase shifter. This 1/4 divided output is derived from pin 31 and compared with the output of fsc VCO in IC1004 in the phase comparator in IC1008. The resultant output corrects the error of the 4 fsc VCO.



(A) DIGITAL ENCODER PRINCIPLE



(B) fsc VCO/ENCODER CIRCUIT

Fig. 3-122 Digital Encoder

3-14-8 D/A converter/NTSC modulator circuits (Fig.3-123)

Fig.3-123 shows the processing circuit which returns the three signals, Y, R-Y and B-Y, converted in parallel, to the original analog Video signal. This circuit consists of IC1006 and IC1008 which D/A convert the two signals and limit their frequency bands, IC1004 which mixes the analog-converted luminance and color-difference signals and IC1002 which clamps the resultant mixed video signal. IC1006 inputs the digital Y signals via pins 10 - 17 and converts the digital signals quantized to 6 bits to an analog signal using the exclusive D/A (Digital/Analog) converter.
The 3 MHz lowpass filter (CP1103) at pin 18 limits the D/A converted Y signal to that specified frequency band.
The digital color-difference signals are D/A converted by IC1008 and limited to the specified frequency band by the 3 MHz BPF consisting of C1090, L1010 and RT1003.
The bandwidth limited Y signal and C signal are applied to pins 16 and 17 of Y/C mixer IC1004 respectively. The mixed signal is output from pin 14 and applied to output switch IC1002. The SUB BPA in IC1004 is a chroma level controller. In the normal mode, the output controlled by the SUB BPA to a fixed level is applied to the mixer, but when no signal is output to the main screen, the internal switch is set to NO VIDEO side by the control signal from pin 15 and the SUB BPA is bypassed.

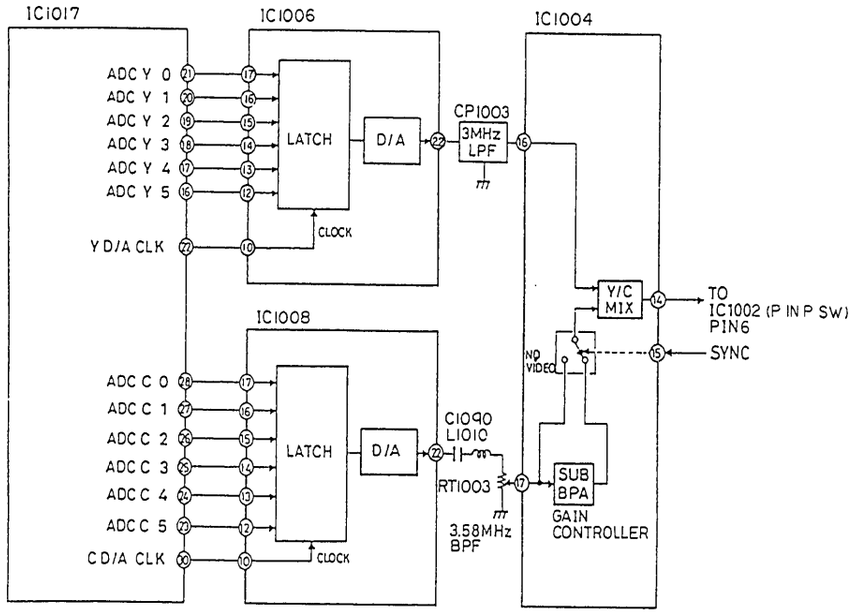


Fig. 3-123 D/A Converter/NTSC Modulator

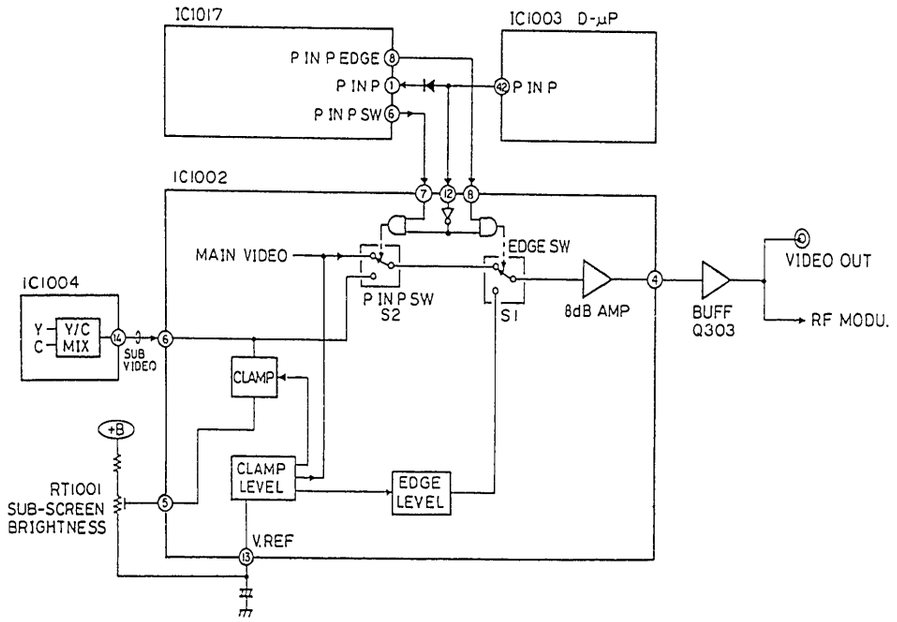


Fig. 3-124 P IN P SW/P IN P Edge SW Circuit

3-14-9 P in P SW/P in P EDGE SW circuit (Fig.3-124)

Fig.3-124 shows a circuit which replaces the main screen video signal with the video signal of the sub-screen with the time axes shortened and its edge signal.
IC1002 uses the clamper (CLAMP) and aligns the sync tip of the sub-screen with that of the main screen to match the tone correctly when the same pattern is selected for the main and sub-screens.
The CLAMP setting voltage is obtained by the clamp level control circuit and brightness control (RT1001). The output of the clamp level control circuit is applied to the main video and edge level control circuits.
This circuit consists of a switch group in IC1002. The P in P switch performs replacement of the video signal and the edge switch generates an edge signal.

IC1002 receives the main-screen composite video signal (MAIN VIDEO) and the sub-screen composite video signal (SUB VIDEO) supplied at pin 5.
Then IC1002 selects one of them according to the one of the 4 corners of the main screen in which the sub-screen is to be displayed (determined by the P in P controller) and then outputs it at pin 4.
The P in P controller determines the read timing of the sub-screen data and the replacement timing of the video signals using the data of the sub-screen position in the main screen commanded by the operator and the sync signal separated from the main-screen video signal.
The P in P controller generates two video signal replacement control signals (P in P SW, P in P EDGE SW) and outputs them at pin 6 and 8.
The P in P SW signal at pin 6 drives the P in P switch in IC1002 to determine the timing of frame the sub-screen.

The P in P EDGE SW signal at pin 8 drives the edge switch in IC1002 to determine the timing of frame the sub-screen with edge lines. The widths of edge lines are determined as 1/fH vertical and 1/fsc horizontal.
The DC edge level is obtained from the edge level control circuit. The edge level control circuit is interlocked with the output of the clamp level control circuit and applies edges with a certain level to the edge switch from the main video clamp level control circuit.
The output of the edge switch is applied to pin 4 via the 8-dB amplifier.
The video signal at pin 4 of IC1002 which is obtained by framing the sub-screen in the main screen is supplied to the RF modulator and video output jack via the buffer (Q303).

3-15. Main IC Pin Specifications, Abbreviation List

(1) Digital up IC1003
(2) Trick play controller IC1015
(3) Multi-controller IC1016
(4) P in P controller IC1017
(5) Abbreviations for Digital Video Block

3-15-1 Digital µP (IC1003) Pin Specifications

Pin No.	I/O	Active Level	Abbreviation	Function
1	I	H	TRANSIENT	Inputs "Hi" during mode transition. The trailing edge of this signal releases the memory hold.
2	I	H	CM BRAKE	Capstan motor brake pulse (active "Hi") input.
3	I		P in P POSIT.	Inputs "Hi" pulses by the number of P in P positions stored in the system control µP when the P in P mode is entered.
4	I	H	DA4	Hi: DA 4-head system, Lo: System other than DA 4-head
5	O	H	MOSAIC	Hi: MOSAIC mode, Lo: Modes other than MOSAIC
6	O	H	PAINT	Hi: PAINT mode, Lo: Modes other than PAINT
7	O	H	MOSAIC SIZE	Hi: When MOSAIC size is large and in P in P REV trick play, Lo: In modes other than the above
8	O	H	PAINT BIT	Hi: Rough (fixed to 3 bits) Lo: Fine (fixed to 2 bits)
9	O	H	PB	Hi: During play and trick play, Lo: In modes other than play and trick play
10	O	H	SLOW	Hi: During still and slow, Lo: In modes other than still and slow
11			NC	
12			NC	
13	O	H	X2 SPEED	Hi: During X2 SPEED play, Lo: In modes other than quick
14	O	H	SEARCH	Hi: During search, Lo: In modes other than search
15	I		RESET	"Hi" input resets the µP.
16			OSC 1	Ceramic capacitor connection pin for oscillating system clock
18			OSC 2	Ceramic capacitor connection pin for oscillating system clock
17			VCC	Power supply pin
19	I	H/L	SW30	SW30 input
20	I	H/L	W. FINE SLOW	Hi: During W. fine slow with DA4 and S. fine slow with DIG3 Lo: In modes other than above
21	I	H/L	CLOCK (S-T)	Clock input to timer from system control

Pin No.	I/O	Active Level	Abbreviation	Function
22	I	H/L	DATA (S-T)	Data input to timer from system control
23			NC	
24	I	H/L	DATA (T-S)	Data input to system control from timer
25	O	H	REVERSE	Hi: During reverse mode, Lo: In modes other than reverse
26	O	H	TRICK PLAY	Hi: During trick play, Lo: In modes other than trick play
27	O	H	SP	Hi: In SP mode, Lo: In modes other than SP
28	I	H	P in P ZOOM	Not used. Connected to Vss.
29	O	H	FAST SEARCH	Not used. Open
30	O	H	NOISE REDUC.	Not used. Open
31	O	H	DIGITAL REC	Hi: During digital recording, Lo: In modes other than digital recording
32	O	H	SKEW CORRECT	Not used. Open
33	O	H	MEM. STANDBY	Hi: In non-digital mode, Lo: In digital mode
34	O	L	$\overline{\text{MULTI RECALL}}$	Hi: In modes other than MULTI, MULTI RECALL, P in P, Lo: In MULTI, MULTI RECALL, P in P modes
35	O	H	M.W.INH/ MULTI W.PULSE	Hi: In memory hold mode, Lo: Writing-to-memory enable mode
36	O	H/L	TRICK SW	Hi: DIGITAL signal output, Lo: ANALOG signal output
37			GND	GND pin
38			EVENT	Not used. Connected to GND.
39			ø out	Not used. Open
40	O		P in P POSI.	Outputs "Hi" when sub picture is shifted in P in P mode.
41	O	H	P in P INV.	Hi: P in P main/sub inverting mode, Lo: In modes other than inverting mode
42	O	H	P in P	Hi: In T in T mode, Lo: In modes other than T in T
43	O	H	MULTI	Hi: In MULTI mode, Lo: In modes other than MULTI
44			NC	

3-15-2 Trick Play Controller (IC1015) Pin Specifications

Pin No.	I/O	Active Level	Abbreviation	Function
1	I	H/L	PAINT BIT	Controls the steps in the PAINT mode (step removal) Hi: 3 bits, Lo: 4 bits
2	O	H/L	$\overline{\text{D/A CLOCK}}$	Inversion signal of D/A CLOCK pin 92. Not used.
3	O	L	ART V. SYNC	Artificial V sync output. This pin outputs an artificial V sync pulse in the trick play mode. Not used.
4	O	L	A/D SW	Sub picture (P in P) writing control output. Performs controls so that fields with too much noise are not written as sub pictures to perform noiseless sub picture trick play. Not used.
5	I	-	3 Fsc IN	Reference clock (3 fsc) input
6	I	-	DL CLOCK	Delayed clock (3 fsc) input. Delay signal (30 nsec) of 3 Fsc (pin 5)
7	O		ART V. T1	Phase MM trigger output which triggers the external phase setting MM.
8	I		ART V. Q1	Variable artificial V sync phase input. Sets the phase of artificial V sync pulse.
9	O		ART V. T2	Artificial V sync trigger output which triggers the artificial V sync setting MM.
10	I	H	ART V. Q2	Artificial V sync input. Inputs artificial V sync pulse from the artificial V sync MM.
11	O	H	TRICK PLAY	Video signal switching output. Controls switching between normal video signal and trick play video signal.
12	I	L	MEM. STANDBY	Initializes the trick play controller. Resets the internal circuits of the trick play controller to set them to the standby state.
13	I	H	WR. INH	Memory hold signal. Holds the data in the memory.
14	I	H	MOSAIC	MOSAIC mode input. Sets the trick play controller to the MOSAIC mode.
15	-	-	GND	IC ground pin
16	I	H	PAINT	PAINT mode setting input
17	I	H	SEARCH	Search mode setting input
18	I	H	REVERSE	Reverse mode setting input
19	I	H	X2 SPEED	X2 speed mode setting input
20	I	H	SLOW	Slow mode setting input
21	I	H	PLAYBACK	Play mode setting input

Pin No.	I/O	Active Level	Abbreviation	Function
22	I		MAIN H. SYNC	MAIN H. SYNC input. Inputs the H SYNC-AFC signal of the output video signal side. The artificial H. SYNC is produced from this signal.
23	O	-	Fsc OUT	Signal obtained by dividing 3 Fsc (pin 5) by 3. Signal to compare the phase with the subcarrier.
24	I	H/L	SIZE	Controls the data repeating number in the MOSAIC mode to change the size of mosaic. Lo: 2 cycles of fsc in horizontal, 4H repeated in vertical Hi: 4 cycles of fsc in horizontal, 8H repeated in vertical
25	I		SUB V. SYNC	SUB V. SYNC input which becomes a start trigger in PLAY, PAINT and MOSAIC modes.
26	I		SUB. C. SYNC	SUB picture composite sync signal (input-side video signal). This becomes a reference signal for the PAINT and MOSAIC inhibit gates and repeating.
27	I		REF30	External sync signal input. When TRICK (pin 33) is "Lo", the leading edge of REF30 (this pin) synchronizes the memory reference signal.
28	I		SW30	SW30Hz input. This becomes the start trigger for play.
29	I	H/L	FIELD SW	Designates the write field in the slow mode.
30	I	H/L	SP	Hi: SP mode play, Lo: EP mode play
31	O		MEM. REF30	Memory reference signal output. The phases of the servo IC phase reference signal and this signal are compared to synchronize the memory output signal and playback signal.
32	I	H	P in P INV.	P in P main/sub inverting (sub picture play) mode input. When P in P INV. (pin 32) is "Hi" and P in P (pin 34) is "Hi", the trick play controller does not work for trick play. The P in P write inhibit signal, A/D SW (pin 4) is also output.
33	I	H	TRICK SW	Trick play mode input. This signal sets the trick play controller to the trick play mode.
34	I	H	P in P	P in P mode input
35	I	H/L	X9	Search double speed switching input

	SP	LP	EP
Hi	X9	X9	X9
Lo	X3	X6	X9

Pin No.	I/O	Active Level	Abbreviation	Function
36	I		SKEW. EN.	Not used. Grounded
37	I	H/L	D/A SW	D/A converter operating control pin. When this pin is "Hi", the D/A converter output is connected to the P in P controller (Pins 95 (Y5) to 100 (Y0) are open), and when this pin is "Lo", it is connected to the trick play controller.
38	-	-	TEST	GND
39	-	-	TEST	GND
40	I	H/L	SHIFT	Artificial V. SYNC phase control pin. When this pin is "Hi", the artificial V. SYNC is in phase with the edge of H. SYNC, and when it is "Lo", the phase of artificial H. SYNC is shifted by 1/4H from the edge of H. SYNC as a countermeasure for digital TVs.
41	-	-	Vcc	Power supply pin
42-45, 50-53, 58-61, 75-78				Coded picture information writing outputs and reading inputs
42	I/O	H/L	MPX VIDEO 15	Data to be written and read to/from the memory
43	I/O	H/L	MPX VIDEO 14	
44	I/O	H/L	MPX VIDEO 13	
45	I/O	H/L	MPX VIDEO 12	
46	-	-	TEST	GND
47	-	-	$\overline{\text{TEST}}$	Connected to Vcc.
48	-	-	TEST	GND
49	O	-	TEST	Open
50	I/O	H/L	MPX VIDEO 11	Memory writing/reading data
51	I/O	H/L	MPX VIDEO 10	
52	I/O	H/L	MPX VIDEO 09	
53	I/O	H/L	MPX VIDEO 08	
54	-	-	TEST	GND
55	-	-	TEST	GND
56	O		SERVO SET	Servo IC synchronizing signal. When TRICK SW (pin 33) is "Hi", this outputs a pulse indicating the memory reference phase. The pulse is input to the servo IC which has an external synchronization function to synchronize the playback signal and memory output signal. Not used.
57	-	-	$\overline{\text{TEST}}$	Connected to Vcc.

Pin No.	I/O	Active Level	Abbreviation	Function
58	I/O	H/L	MPX VIDEO 07	Memory writing/reading data
59	I/O	H/L	MPX VIDEO 06	
60	I/O	H/L	MPX VIDEO 05	
61	I/O	H/L	MPX VIDEO 04	
62	O	H/L	TEST	Open
63, 64, 66-70, 72				Memory address data outputs (ADDRESS 0 - 7)
63	O	H/L	ADDRESS 7	Address data
64	O	H/L	ADDRESS 4	
65	-	-	GND	Grounds the IC
66	O	H/L	ADDRESS 3	Address data is divided into row and column, each of which consists of 8 bits. Writes and reads the trick play picture data (MPX VIDEO 00 - 15) to/from the address in the memory which correspond to the address codes designated by the following. ° Row address: Fall of $\overline{\text{RAS}}$ (pin 71) ° Column address: Fall of $\overline{\text{CAS}}$ (pin 74)
67	O	H/L	ADDRESS 5	
68	O	H/L	ADDRESS 2	
69	O	H/L	ADDRESS 6	
70	O	H/L	ADDRESS 1	
71	O		$\overline{\text{RAS}}$	Row address designating output. Designates the memory row address to write and read the trick play picture data (MPX VIDEO 00 - 15).
72	O	H/L	ADDRESS 0	Address data
73	O	L	$\overline{\text{WE}}$	Trick play picture data writing control output
74	O		$\overline{\text{CAS}}$	Column address designating output
75	I/O	H/L	MPX VIDEO 03	Data to be written and read to/from the memory
76	I/O	H/L	MPX VIDEO 02	
77	I/O	H/L	MPX VIDEO 01	
78	I/O	H/L	MPX VIDEO 00	
79	O	H/L	$\overline{\text{DT}}$	Data transfer/read mode control input. Determines the memory data output mode together with the RAS output (pin 71). When this pin is "Lo" at the fall of RAS, the memory enters the data transfer mode, and when it is "Hi", the memory enters the data read mode.
80	I/O	H/L	D 03	Picture data to be written and read to/from the memory when quantization is 7-bit. Not used. Grounded via resistors.
81	I/O	H/L	D 02	
82	I/O	H/L	D 01	
83 - 88				6-bit digital picture data transferred from the A/D converter

Pin No.	I/O	Active Level	Abbreviation	Function
83	I	H/L	ADC I5	6-bit digiral picture data
84	I	H/L	ADC I4	
85	I	H/L	ADC I3	
86	I	H/L	ADC I2	
87	I	H/L	ADC I1	
88	I	H/L	ADC I0	
89	O	H/L	$\overline{DT}$	Same as $\overline{DT}$ (pin 79). Used when memories in other memory control ICs are used in common. Not used.
90	O	H/L	A/D CLOCK	Outputs an A/D converter operation control clock signal (3 fsc).
91	-	-	Vcc	Power supply pin
92	O	H/L	D/A CLOCK	Outputs a D/A converter operation control clock signal (3 fsc).
93	I	H/L	AD 0	Inputs LSB picture data from the A/D converter when quan tization is 7-bit. Not used. Grounded
94-100				Quantized trick play picture data output ports
94	O	H/L	DA 0	Quantized trick play picture data (LSB) output port with 7-bit quantization. Not used. Open
95	O	H/L	DAC Y5	Picture data outputs of 6 bits processed by the trick play controller. Transferred to the D/A converter.
96	O	H/L	DAC Y4	
97	O	H/L	DAC Y3	
98	O	H/L	DAC Y2	
99	O	H/L	DAC Y1	
100	O	H/L	DAC Y0	

3-15-3 Multi-controller (IC1016) Pin Specifications

Pin No.	I/O	Active Level	Abbreviation	Function
1	O	H	CLAMP (A/D)	Clamp timing output. Determines the clamp timing of the R-Y and B-Y signals before being A/D converted to align the reference signals of the R-Y and B-Y signals after NTSC demodulation and before modulation.
2	O	H	BLP	Blanking signal output
3	I	H	WR. PULSE	Write control pulse input. Goes "Hi" and renews the picture position due to the first input of write vertical sync signal to start writing (one picture moving). Goes "Lo" and renews the picture position due to the first input of write vertical sync signal to stop writing (with all pictures still).
4	O	H	MPX SW B-Y	Multiplexer drive outputs. Selects the sub video signal separated into luminance and color difference signals by time-sharing, by driving the switches corresponding to each signal. ° Y SW supplies the Y signal to the A/D converter once per three horizontal scannings in its horizontal scanning period. ° B-Y SW and R-Y SW supply the B-Y and R-Y signals alternately to the A/D converter in the horizontal scanning period before the Y signal is sampled.
5	O	H	MPX SW R-Y	
6	O	H	MPX SW Y	
7	-	-	$\overline{TEST}$	Fixed to "Hi"
8	O	H	EDGE OUT	Edge signal output
9	O	H/L	ADC C5	6-bit quantized digital color-difference signals (C0 - C5) output ports. These output the digital color-difference signals quantized to 6 bits which were read from memory. The R-Y and B-Y signals read from memory are converted to modulated chroma signals which are quadrature modulated in the multi-controller and are output.
10	O	H/L	ADC C4	
11	O	H/L	ADC C3	
12	O	H/L	ADC C2	
13	O	H/L	ADC C1	
14	O	H/L	ADC C0	
15	-	-	GND	Ground pin
16	O	H/L	Fsc OUT	Outputs a signal obtained by dividing 4 fsc by 4. The output of pin 16 (fsc out) obtained by dividing the 4 fsc VCO output by 4 and color sub-carrier are phase compared to match the phases of pin 30 (RC. 4 fsc) and color subcarrier (fsc), and the 4 fsc VCO is controlled.
17	-	-	$\overline{TEST}$	Fixed to "Hi"

Pin No.	I/O	Active Level	Abbreviation	Function
18	O	H/L	ADC Y5	6-bit quantized digital Y signals (Y0 - Y5) output ports. These output the digital Y signals quantized to 6 bits which were read from the memory. same as C0 - C5.
19	O	H/L	ADC Y4	
20	O	H/L	ADC Y3	
21	O	H/L	YDC Y2	
22	O	H/L	YDC Y1	
23	O	H/L	YDC Y0	
24	I	H	TEST	Test mode/picture vertical position adjustment control input.
25	I	H	MMQ	Input to adjust the picture horizontal position. Inputsthe signal which obtained by delaying pin 16 (MMT) using the MM.
26	O	H	MMT	Picture horizontal position adjustment output
27	-	-	TEST	GND
28	O	H/L	Y D/A CLOCK	Y. D/A converter operation control clock output (4 fsc)
29	-	-	TEST	Open
30	I	H/L	RC. 4 fsc	Read clock input (4 fsc)
31	I	H	INT	Initializing mode/picture vertical position adjustment control input
32	O	H/L	C. D/A CLOCK	C. D/A converter operation control clock output (4 fsc)
33	-	-	-	Not connected.
34	I	H/L	IC5	These input the 6-bit quantized digital color-difference signals read from the memory.
35	I	H/L	IC4	
38	I	H/L	IC3	
39	I	H/L	IC2	
40	I	H/L	IC1	
42	I	H/L	IC0	
36	O	H/L	OC5	These output the 6-bit quantized digital color-difference signals written to the memory.
37	O	H/L	OC4	
43	O	H/L	OC3	
44	O	H/L	OC2	
45	O	H/L	OC1	
46	O	H/L	OC0	

Pin No.	I/O	Active Level	Abbreviation	Function
41	-	-	VCC	Power supply pin
47	I	H/L	IY5B	6-bit quantized digital luminance signals read from the memory. 2 branches (A/B)
48	I	H/L	IY5A	
49	I	H/L	IY4A	
50	I	H/L	IY4B	
55	I	H/L	IY3A	
56	I	H/L	IY3B	
57	I	H/L	IY2A	
58	I	H/L	IY2B	
64	I	H/L	IY1A	
66	I	H/L	IY1B	
67	I	H/L	IY0A	
68	I	H/L	IY0B	
51	O	H/L	OY5B	6-bit quantized digital luminance signals written to the memory. 2 branches (A/B)
52	O	H/L	OY5A	
53	O	H/L	OY4B	
54	O	H/L	OY4A	
57	O	H/L	OY3B	
60	O	H/L	OY3A	
61	O	H/L	OY2B	
62	O	H/L	OY2A	
67	O	H/L	OY1B	
70	O	H/L	OY1A	
71	O	H/L	OY0B	
72	O	H/L	OY0A	
63	O	H/L	SC2	Outputs a clock signal to read data from the memory.
73	O	H/L	SC1	Outputs a serial clock (SC) signal, equivalent to fsc,which is necessary to read data on the line memory buffer in the memory.
65	-	-	GND	GND
74	-	-		Not connected.

Pin No.	I/O	Active Level	Abbreviation	Function
75	I	H/L	MPX VIDEO I5	These input the 6-bit digital picture data supplied from the A/D converter.
76	I	H/L	MPX VIDEO I4	
77	I	H/L	MPX VIDEO I3	
78	I	H/L	MPX VIDEO I2	
79	I	H/L	MPX VIDEO I1	
80	I	H/L	MPX VIDEO I0	
81	O	H/L	A/D CLOCK	Outputs a A/D converter clock signal (2/3 fsc)
82	O	L	$\overline{DT2}$	Data transfer mode/read mode control output
94	O	L	$\overline{DT}$	Determines the memory data output mode together with the output of pin 96 ($\overline{RAS}$). When the output level of this pin goes: ° "Lo", the memory enters the data transfer mode. ° "Hi", the memory enters the data read mode. In the data transfer mode, 1H-component data from the memory cell array is transferred to the memory buffer. In the data read mode, the 1H-component data on the memory buffer is output for each bit (row), synchronized with the serial clock (SC: pins 63 and 73).
83	O	-	C. LEVEL	Output for the color-difference signal feedback clamp
84	O	H/L	ADDRESS 0	Memory address data outputs (A0 - 7). The address data is divided into rows and columns each of which consists of 8 bits. The picture data is written to the address in the memory according to the address code designated by the following. ° Row address: Fall of pin 96 ($\overline{RAS}$) ° Column address: Fall of pin 95 ($\overline{CAS}$)
85	O	H/L	ADDRESS 1	
86	O	H/L	ADDRESS 6	
87	O	H/L	ADDRESS 2	
88	O	H/L	ADDRESS 5	
89	O	H/L	ADDRESS 3	
90	O	H/L	ADDRESS 4	
92	O	H/L	ADDRESS 7	
91	I	-	Vcc	Power supply pin
93	O	L	$\overline{WE}$	Picture data write control output
95	O		$\overline{CAS}$	Column address designation output. This designates the column address in the memory into which picture data is written and also times writing. The digital picture data is written to the memory at the fall.
96	O		$\overline{RAS}$	Row address designation output. This designates the row address in the memory into which picture data is written.
97	I	H	SUB V. SYNC	Vertical sync signal of the picture to be written
98	I	H	SUB H. SYNC	Horizontal sync signal of the picture to be written
99	I	H	MULTI	MULTI mode input. This input sets the multi-controller to the MULTI mode and makes the output ports of the multi-controller active.
100	I	H/L	WC. 4 Fsc	Clock input (4 fsc) for writing

3-15-5 ABBREVIATIONS FOR DIGITAL VIDEO BLOCK

ADC, A/D, AD	Analog to Digital Coversion
ART. V.	Artificial Vertical Sync Signal
BGP	Burst Gate Pulse
BLP	Blanking Pulse
BPA	Band Pass Amp
CAS	Column Address Strobe
C. BLANK	Chroma Blanking
C. LEVEL	Clamp Level
C. SYNC	Composite Sync Signal
CYL. REF30	Cylinder Reference 30Hz
DA4	Double Azimuth 4-Head System
DAC, D/A, DA	Digital to Analog Conversion
DIG. 3	Digital 3-Head System
DL	Delayed ...
DRAM	Dynamic Random Access Memory
DT	Data Transfer
F. SEARCH	Fast Speed Search
MEM ...	Memory ...
MEM VIDEO	Memorized Video
MMQ/MMT	Monostable Multivibrator Output/Trigger Input
MPX	Multiplexer
MULTI	Multiple Picture
N. REDUC.	Noise Reduction
P in P	Picture in Picture
RAS	Row Address Strobe
RC	Reading Clock
REF30	Reference 30Hz from Servo Circuit
R/W, RW30	Read Write, Read Write 30Hz
SC	Serial Control Clock
SO, SOE	Serial Out, Serial Out Enable
T in T	TV in TV
WC	Write Clock
WE	Write Enable
W. FINE SLOW	Double Field Fine Slow
WR. ...	Write ...

3-15-4 P in P Controller (IC1017) Pin Specifications

Pin No.	I/O	Active Level	Abbreviation	Function
1	I	Hi	P in P	P in P mode input. This input sets the P in P to the P in P mode and enables the output ports of the controller.
2	O	Hi	B-Y MPX SW	Multiplexer drive outputs. Drive the switches corresponding to the luminance and color-difference signals separated from the sub screen video signal to select the signals using time-sharing. o The Y MPX SW supplies the Y signal to the A/D converter once for each three horizontal scanning lines during that horizontal scanning period. o The B-Y and R-Y MPX SWs supply the B-Y and R-Y signals alternately to the A/D converter in the next horizontal scanning period in which the Y signal is to be sampled.
3	O	Hi	R-Y MPX SW	
4	O	Hi	Y MPX SW	
5	-	-	TEST	GND
6	O	Hi	P in P SW	Sub-screen position output. The output timing is determined by the position of the corner of the main screen in which the sub-screen is framed and the sync signal separated from the main-screen video signal.
7	-	-	CLAMP	Aligns the pedestal levels of the main and sub-screens after D/A conversion. (Not used because sync tip clamp is performed in this model.)
8	O	Hi	P in P EDGE	Edging control output. The timing of edging is determined by the position of sub-screen and main-screen sync signals.
9	I	Hi	MEMORY PLAY	Main-screen trickplay mode input.
10	I	Hi	MAIN V.SYNC	Main-screen vertical sync signal input. Times the change of field when reading the digital sub-screen data from the P in P memory.
11	I	Hi	MAIN H.SYNC	Main-screen horizontal sync signal input. Times to change of row address when reading the digital sub-screen data from the P in P memory.
12	I	Hi	MULTI	Multi-mode control input.
13	O	Lo	$\overline{\text{RCC}}$ (Read Clock Clear	Read clock signal generator reset output. Stops the read clock signal generator to inhibit reading from the P in P memory for approx. 3 µs when the main-screen enters the horizontal sync period.
14	I	Hi/Lo	RC (Read Clock)	Read clock signal input. Inputs a clock signal equivalent to 4.5fsc necessary to read digital sub-screen data from the P in P memory from the clock signal generator.
15	-	-	GND	IC ground terminal

Pin No.	I/O	Active Level	Abbreviation	Function
16-22			6-bit quantized digital Y signal (A/D C Y0 - Y5) output ports.	
16	O	Hi/Lo	A/D C Y5	Output ports of digital Y signal quantized to 6 bits and read from the memory. Same as A/D C (C0-C5).
17	O	Hi/Lo	A/D C Y4	
18	O	Hi/Lo	A/D C Y3	
19	O	Hi/Lo	A/D C Y2	
20	O	Hi/Lo	A/D C Y1	
21	O	Hi/Lo	A/D C Y0	
22	O	Hi/Lo	Y D/A CLOCK	Y signal D/A converter operation control clock output (2 fsc)
23-28			6-bit quantized digital color-difference signal (A/D C C0 - C5) output ports.	
23	O	Hi/Lo	A/D C C5	Output ports of color-difference signals obtained by quantizing 4-bit data read from the memory again to the original 6 bits. The R-Y and B-Y signals read from the P in P memory are quadrature 2-phase modulated in the P in P controller to be converted to modulated chroma signals and are output.
24	O	Hi/Lo	A/D C C4	
25	O	Hi/Lo	A/D C C3	
26	O	Hi/Lo	A/D C C2	
27	O	Hi/Lo	A/D C C1	
28	O	Hi/Lo	A/D C C0	
29	O	-	CLIP	Clip pulse output. Outputs a pulse while a sub-screen is displayed to prevent the level from dropping below the pedestal level. (not used)
30	O	Hi/Lo	C D/A CLOCK	Chroma signal D/A converter operation control clock output.
31	O	-	fsc	Outputs a signal obtained by dividing the 4fsc signal by four. To match the phases of the signal at pin 33 (4fsc) and color subcarrier (fsc), the output at pin 31 (fsc) obtained by dividing the 4fsc VCO output by four and the color subcarrier are phase compared and the 4fsc VCO is controlled.
32	I	Hi	POSITION ADJ	Controls the presence/absence of sub-screen display position adjustment. Hi: Present
33	I	-	4 fsc	Clock input (4fsc) for digital encoder.
34	-	-	TEST	Not connected.
35-59			Multi-gate array control input/output circuit	
35	I	Lo	M.$\overline{\text{RAS}}$ IN	Row address data writing process mode designation input. Writes at the fall of this input.
36	I	Lo	M.$\overline{\text{CAS}}$ IN	Column address data writing process mode designation input. Writes at the fall of this input.
37	I	Lo	M.DT IN	Data transfer mode/read mode control input.

Pin No.	I/O	Active Level	Abbreviation	Function
38	I	Lo	M.$\overline{WE}$ IN	Data write control input. Writes at the fall.
39	I	Hi/Lo	M.ADRS I7	8-bit address data (ADDRESS I0 - I7) input ports
40	I	Hi/Lo	M.ADRS I4	
41	-	Hi	+B	
42	I	Hi/Lo	M.ADRS I3	
43	I	Hi/Lo	M.ADRS I5	
44	I	Hi/Lo	M.ADRS I2	
45	I	Hi/Lo	M.ADRS I6	
46	I	Hi/Lo	M.ADRS I1	
47	I	Hi/Lo	M.ADRS I0	
48	O	Hi/Lo	M.ADRS O7	8-bit address data (ADDRESS O0 - O7) output ports
49	O	Hi/Lo	M.ADRS O4	
50	O	Hi/Lo	M.ADRS O3	
51	O	Hi/Lo	M.ADRS O5	
52	O	Hi/Lo	M.ADRS O2	
53	O	Hi/Lo	M.ADRS O6	
54	O	Hi/Lo	M.ADRS O1	
55	O	Hi/Lo	M.ADRS O0	
56	O	Lo	M.RAS OUT	Row address data writing process mode designation output. Writes at the fall of this output.
57	O	Lo	M.$\overline{CAS}$ OUT	Column address data writing process mode designation output. Writes at the fall of this output.
58	O	Lo	M.$\overline{DT}$ OUT	Data transfer mode/read mode control output.
59	O	Lo	M.$\overline{WE}$ OUT	Data write control output. Writes at the fall.
60-67, 69			P in P memory address data outputs (ADDRESS 0 - 7)	
60	O	Hi/Lo	ADRS 7	Address data is divided into rows and columns, each consisting of 8 bits. Sub-screen data (MPX VIDEO 0 - 3: pins 72 - 75) is written to the address in memory according to the address code designated by the following: ° Row address: Fall of pin 68 ($\overline{RAS}$) ° Column address: Fall of pin 71 ($\overline{CAS}$)
61	O	Hi/Lo	ADRS 4	
62	O	Hi/Lo	ADRS 3	
63	O	Hi/Lo	ADRS 5	
64	O	Hi/Lo	ADRS 2	
65	-	Lo	GND	
66	O	Hi/Lo	ADRS 6	
67	O	Hi/Lo	ADRS 1	
69	O	Hi/Lo	ADRS 0	

Pin No.	I/O	Active Level	Abbreviation	Function
68	O		$\overline{RAS}$ (ROW ADDRESS STROBE)	Row address designation output. Designates the row address in memory to which sub-screen data is written.
70	O	Lo	$\overline{WE}$ (WRITE ENABLE)	Sub-screen data write control output.
71	O		CAS (COLUMN "fsc" STROBE)	Column address designation output. Designates the column address in memory to which sub-screen data is written and times writing. The digital sub-screen data is written to the P in P memory at the fall.
72-75			4-bit digital sub-screen data write output. (MPX VIDEO O0 - O3)	
72	O	Hi/Lo	MPX V O1	4-bit digital sub-screen data to be written to the P in P memory.
73	O	Hi/Lo	MPX V O2	
74	O	Hi/Lo	MPX V O0	
75	O	Hi/Lo	MPX V O3	
76	O	Lo	$\overline{DT}$ (DATA TRANSFER	Data transfer mode/read mode control output. Determines the data output mode of the P in P memory in combination with the output at pin 68 ($\overline{RAS}$). At the fall of the output at pin 68, when the output goes: ° "Lo", the P in P memory enters the data transfer mode. ° "Hi", the P in P memory enters the read mode. In the data transfer mode, the 1H-component data from the memory cell array is transferred to the memory buffer. In the read mode, the 1H-component data from the memory buffer is output as 1 bit (1 column), synchronized with serial clock (SC: pin 81).
77-80			4-bit read inputs (MEMORY VIDEO 0 - 3)	
77	I	Hi/Lo	MEM VIDEO 1	4-bit digital sub-screen data read from the P in P memory.
78	I	Hi/Lo	MEM VIDEO 2	
79	I	Hi/Lo	MEM VIDEO 0	
80	I	Hi/Lo	MEM VIDEO 3	
81	O	Hi/Lo	SC (SERIAL CLOCK)	Clock signal output for reading from the P in P memory. Outputs serial clock (SC) equivalent to 4.5fsc necessary to read data from the line memory buffer in the P in P memory. Outputs only during the sub-screen display period.
82	I	Lo	MAIN CONT	Sub-screen display control output when no main-screen signal is present. Lo: Sub-screen display

Pin No.	I/O	Active Level	Abbreviation	Function
83	I	Hi/Lo	MPX V. I5	Input 6-bit digital sub-screen data supplied from the A/D converter.
84	I	Hi/Lo	MPX V. I4	
85	I	Hi/Lo	MPX V. I3	
86	I	Hi/Lo	MPX V. I2	
87	I	Hi/Lo	MPX V. I1	
88	I	Hi/Lo	MPX V. I0	
89	I	Hi/Lo	A/D SW	A/D converter operation control input. Hi: The A/D converter is connected to the trickplay gate array. Lo: The A/D converter is connected to the P in P gate array.
90	O	Hi/Lo	A/D C CLOCK	Clock signal (4fsc) output for the A/D converter.
91	-	Hi	+B	Gate array power supply pin.
92	I	Hi/Lo	$\overline{WC}$ (Write Clock)	Clock signal equivalent to 4fsc necessary to write digital sub-screen data to the P in P memory. Inputs from the RC clock signal generator. In the gate array, ° It is divided by four to generate $\overline{RAS}$ and $\overline{CAS}$ designating addresses. ° It becomes the operation clock of the A/D converter (A/D C clock in same phase.
93	O	Lo	$\overline{WCC}$ (Write Clock Clear)	Write clock signal generator reset output. Stops the WC clock signal generator to inhibit to the P in P memory for approx. 3 µs when the original sub-screen picture enters the horizontal sync period.
94	I	Hi	RCA	Switches the sub-screen output position.
95	O	-	C.LEVEL	Color-difference signal feedback clamp output.
96	O	Hi	CLAMP (A/D)	Clamp timing output. Determines the clamp timing of the R - Y and B - Y signals before A/D conversion to align the reference voltage of the signals after NTSC demodulation and before NTSC modulation.
97	O	Hi	BLP	Blanking signal output.
98	I	Hi	P IN P POSITION	Sub-screen position change input. Inputs the command that shifts the sub-screen position counterclockwise to another corner of the main screen.
99	I	Hi	SUB V.SYNC	Sub-screen vertical sync signal. — Reference signals to determine the position of picture in the sub-screen.
100	I	Hi	SUB H.SYNC	Sub-screen horizontal sync signal

4. VIDEO CIRCUITS

The video circuits are designed for S-VHS but permit recording and playback in both the S-VHS and standard VHS systems. The VHS HQ system is incorporated and used in recording and playback in the standard VHS mode.

4-1 S-VHS System (Fig. 4-1)

The S-VHS system presents high picture quality with a horizontal resolution of more than 400 lines while maintaining upward compatibility* with standard VHS.

This has been achieved mainly by the addition of subemphasis, changed FM carrier frequency and clip level, S-VHS high-performance tape, and separate Y/chroma input/output (I/O) connector (S Connector).

* Upward compatibility:
A tape recorded using S-VHS cannot be played back by an ordinary standard-VHS VTR.

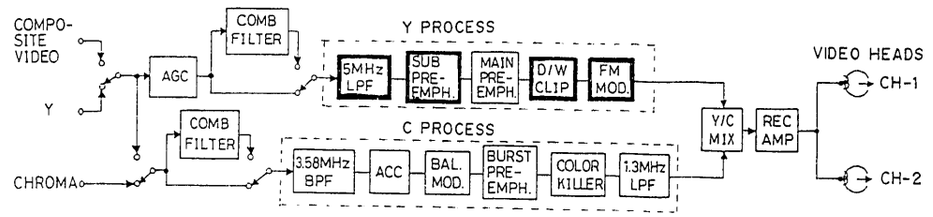


Fig. 4-1a S-VHS System -Record-

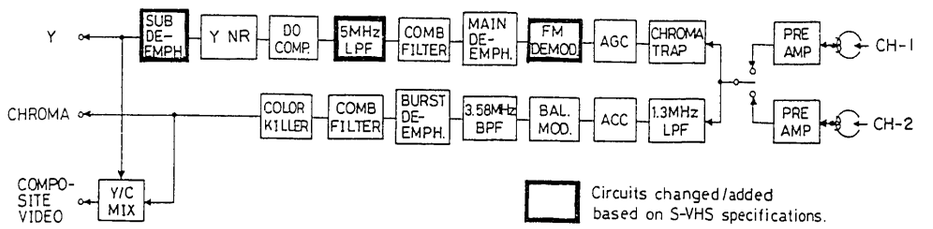


Fig. 4-1b S-VHS System -Playback-

4-1-1 S-VHS high-performance cassette tape (Fig. 4-2)

Cassette:
The dimensions of the cassette are the same as those of the standard VHS cassette, but the S-VHS cassette has an ID hole indicating that the tape is made for S-VHS recording.

An S-VHS VTR records in the S-VHS mode only when a cassette having this ID hole is loaded.

Tape:
The tape itself is high performance tape having a ferric oxide (Fe_2O_3) coating. Output at high frequencies is greatly improved by super-fine particle technology in order to handle the wider frequency range of the luminance signal.

S-VHS high-performance cassettes can also be used in a standard VHS VTR.

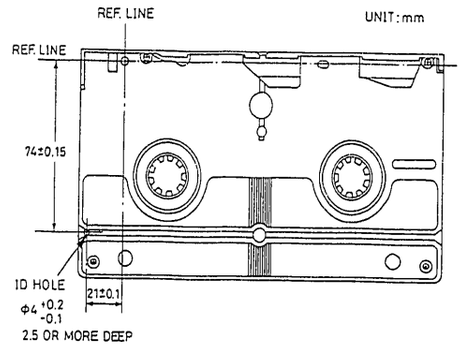


Fig. 4-2 ID Hole in S-VHS Cassette Tape (Standard Cassette)

4-1-2 FM carrier frequency of luminance signal (Fig. 4-3)

	Sync tip	White clip	Deviation	H. Resolution
Normal (HQ)	3.4 MHz	4.4 MHz	1.0 MHz	240 MHz
S-VHS	5.4 MHz	7.0 MHz	1.6 MHz	400 MHz

The range of frequency deviation is expanded to 1.6 MHz with the white peak of the FM luminance signal raised to 7.0 MHz and the sync tip to 5.4 MHz. This increase in the amount of information enables a horizontal resolution of more than 400 lines. Furthermore, the FM carrier frequency is raised to reduce interference with the down-converted chroma signal and to improve crosscolor and moire' interferences.

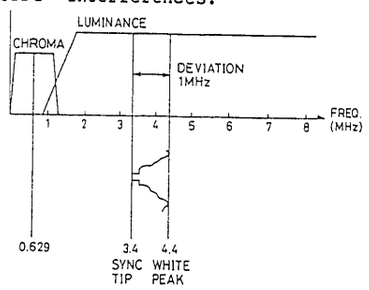


Fig. 4-3a VHS Recording Signal Spectrum

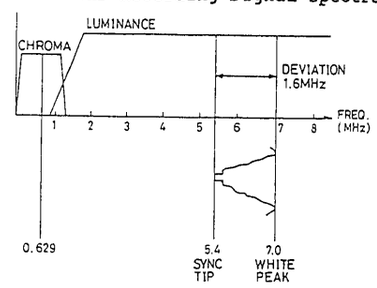


Fig. 4-3b S-VHS Recording Signal Spectrum

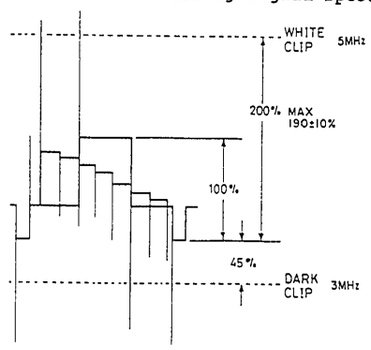


Fig. 4-5a VHS HQ Clip Level

4-1-3 Subemphasis (Fig. 4-4)

The subemphasis circuit before the main emphasis circuit works exclusively for S-VHS. It performs nonlinear emphasis, that is, the amount of emphasis varies with the input level.

Since the FM signal is more susceptible to noise at high frequencies than at low frequencies, low-level high-frequency components are emphasized during recording and the original level is restored during playback. This improves the S/N.

The subemphasis circuit operates in both the SP and EP modes; the dynamic emphasis used in the VHS EP mode is not used in either S-VHS mode.

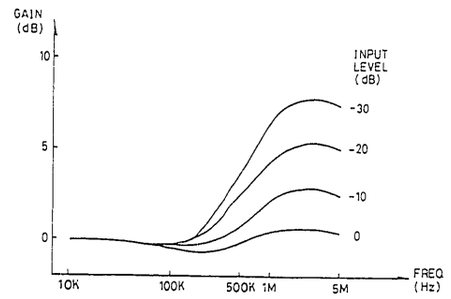


Fig. 4-4 S-VHS Sub Emphasis

4-1-4 Clip level (Fig. 4-5)

	Dark clip	White clip
Normal	45%	180%
HQ	45%	200%
S-VHS	70%	210%

The waveform of the emphasized recording signal will contain over/undershoots. In the S-VHS system, the white clip level is 210% and the dark clip level 70%. This, enabled by improved tape performance, improves pulse response and permits the reproduction of the edges in the picture with higher definition.

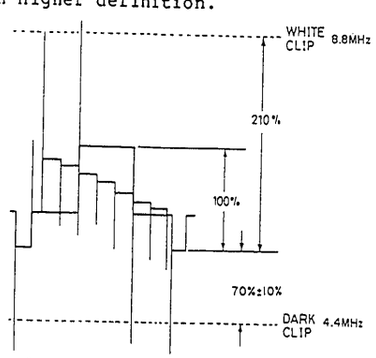
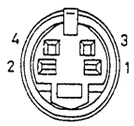


Fig. 4-5b S-VHS Clip Level

4-1-5 Separate Y/C signal input/output connector (S-connector) (Fig. 4-6)

This connector is provided separately from the ordinary NTSC input/output jacks. It outputs the luminance (Y) and chroma (C) signals and inputs separately from each other.

Use of this connector eliminates interference between the luminance and chroma signals and improves dot and crosscolor interferences and, as a result, improves picture quality.



PIN 1: LUMINANCE GND
PIN 2: CHROMA GND
PIN 3: LUMINANCE IN/OUT
1Vp-p 75Ω UNBALANCED
NEGATIVE SYNC
PIN 4: CHROMA IN/OUT
BURST 0.286Vp-p
75Ω UNBALANCED

Fig. 4-6 Separate Y/C In/Out Connector

4-2 S-VHS/VHS Mode Discrimination Circuit (Fig. 4-7)

This circuit comprises IC1204, S-VHS switch (S791) and the ID hole detecting switch (S143) fitted to the mechanism. It sets up the mode during recording and automatically discriminates the mode during playback.

4-2-1 Setting up mode during recording

When an S-VHS cassette is loaded, the S-VHS or standard VHS mode may be selected with the S-VHS switch. When a VHS cassette is loaded, the VHS mode will always be selected.

The logic circuit uses the comparator output to discriminate the mode when the output from the AND circuit is "Hi" and uses the voltage at pin 12 to discriminate the mode when it is "Lo".

During recording, IC1204 pin 16 is "Lo". The logic circuit determines the outputs at pin 9 (S-VHS mode: "Hi") and at pin 7 (VHS mode: "Hi"), depending on the level at pin 12.

With pin 12, the S-VHS switch (S791) and the ID hole detection switch (S143) are connected in series. The logic selects the S-VHS mode when pin 12 is "Hi" and the VHS mode when it is "Lo".

4-2-2 Automatic discrimination of mode during playback

When an S-VHS cassette is loaded, the S-VHS and VHS modes are discriminated by detecting the frequency of the FM signal recorded on the tape. When a VHS cassette is loded, the VHS mode will always be selected. When an FM signal is not detected, the previous mode is held.

When a S-VHS cassette is played back, pins 16 and 4 go "Hi" to disable the input at pin 12.

During playback, IC1204 pin 16 is "Hi" and the input to pin 12 is ignored.

The playback FM signal input to pin 6 is divided into two components. One goes to the S-VHS BPF and the other to the VHS BPF and they are both smoothed. A comparator compares the smoothed level with a reference level and gives the logic circuit information when the smoothed voltage is higher than a reference voltage.

The reference voltage is set to a smoothed voltage so that the FM signal level at pin 6 is 100 mVp-p in order to prevent erroneous operation of the logic

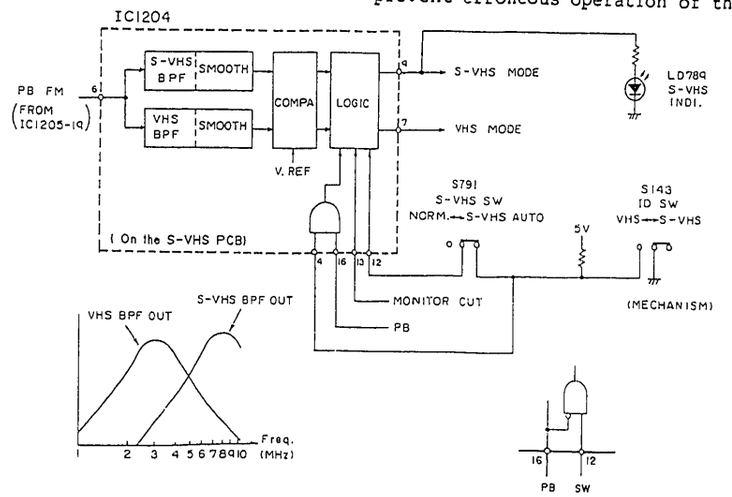


Fig. 4-7 S-VHS/VHS Mode Discrimination

circuit when the FM output has dropped as in the noise band during search. So, when the FM signal level is below 100 mVp-p, the logic circuit does not discriminate the mode but rather holds the previous mode. The previous mode is also held when pin 13 is "Hi".

When a VHS cassette is played back, pins 16 and 4 go "Lo", therefore, the VHS mode is entered forcibly.

4-3 Dual Comb Filter

4-3-1 Operating principle (Fig. 4-8)

In the NTSC color TV signal, chroma and luminance signals are multiplexed by frequency-interleaving and therefore high-frequency components of the luminance signal interfere with the chroma signal, causing dot and crosscolor interference. To attain high resolution, it is required that the chroma signal only may be attenuated without affecting the high-frequency components of the luminance signal and, in order to remove crosscolor interference, the requirement is that the chroma signal does not include any luminacne components.

The dual comb filter separates the chroma and luminance signals whose energy distributions are interleaved with each other.

The chroma subcarrier frequency (fsc) of the NTSC composite video signal is selected as follows.

fsc = 455·fH/2
(fH: horizontal scanning frequency)

As fsc is a multiple of fH/2 raised by the odd number, the phase of fsc inverts for every scanning line. This makes it possible to obtain the luminance component (integral multiple of fH) with the chroma signal canceled, by adding the original signal to the 1H-delayed signal. The chroma component (odd multiple of fH/2) may be obtained with the luminance signal canceled, by subtracting the 1H-delayed signal from the original signal.

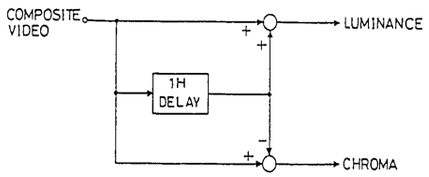


Fig. 4-8 Dual Comb Filter Operation Principle

4-3-2 Operation of the circuit (Fig. 4-9)

The composite video signal A applied to pin 1 will be attenuated at around 3.58 MHz with a 3.58-MHz trap. B is the resulting spectrum. The operational amplifier (op amp) 1 subtracts the signal B from the original signal A to give signal C that rises only near 3.58 MHz.

Signal C is applied to op amps 2 and 3 and to a 1H-delay line. It not only delays the signal C but inverts its phase. As a result, the luminance signal output from the 1H-delay line is in reverse phase to the signal C while the chroma signal is in phase.

Op amp 2 subtracts the 1H-delayed signal from signal C to supply signal D, that has its chroma component canceled, to the mixer. The mixer adds signals B and D to give a wideband luminance signal E having its chroma component canceled, to pin 5. Op amp 3 adds signal C with the 1H-delayed signal to give chroma signal F having its luminance component canceled, to pin 7.

This VTR uses two dual comb filters in the input stage (IC1201 on S-VHS board) of the luminance signal recording circuit and at the output stage (IC1253 on video I/O board) of the digital circuit.

4-4 Feedback Comb Filter (Fig. 4-10)

This VTR uses a feedback comb filter to eliminate crosstalk in the playback chroma signal caused by adjacent tracks. It is basically the ordinary crosstalk-eliminating comb filter but with feedback applied to improve the comb-shaped characteristics.

The playback chroma signal A from IC206 pin 7 is applied to the 1H-delay line and op amps 2 and 3 through op amp 1.

Op amp 2 subtracts the 1H-delayed signal from the original signal to give signal B which rises at odd multiples of fH/2. This is the same as in the ordinary comb filter. The difference is that the feedback comb filter then feeds back the signal that rises at integral multiples of fH to the input.

Op amp 3 adds the original signal to the 1H-delayed signal to give signal C that rises at integral multiples of fH. Signal C is sent back to op amp 1 through the feedback loop beta having its gain adjusted by about 0.7. Op amp 1 subtracts signal C from the input signal. Comb-filter characteristic D having sharp peaks is obtained in this way.

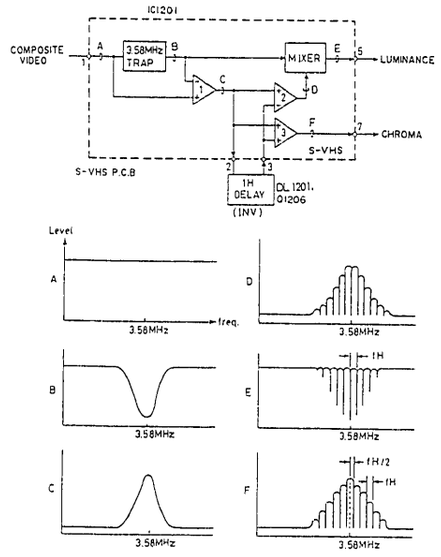


Fig. 4-9A Dual Comb Filter (IC1201)

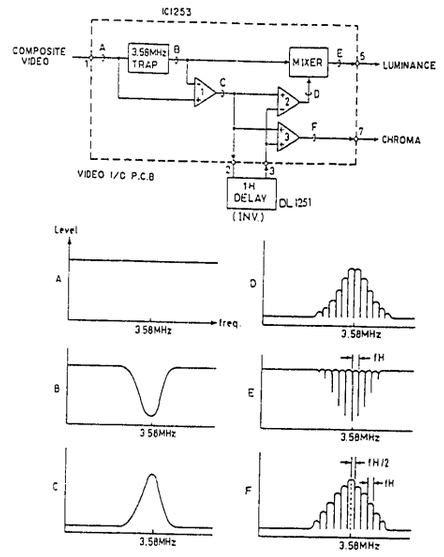


Fig. 4-9B Dual Comb Filter (IC1253)

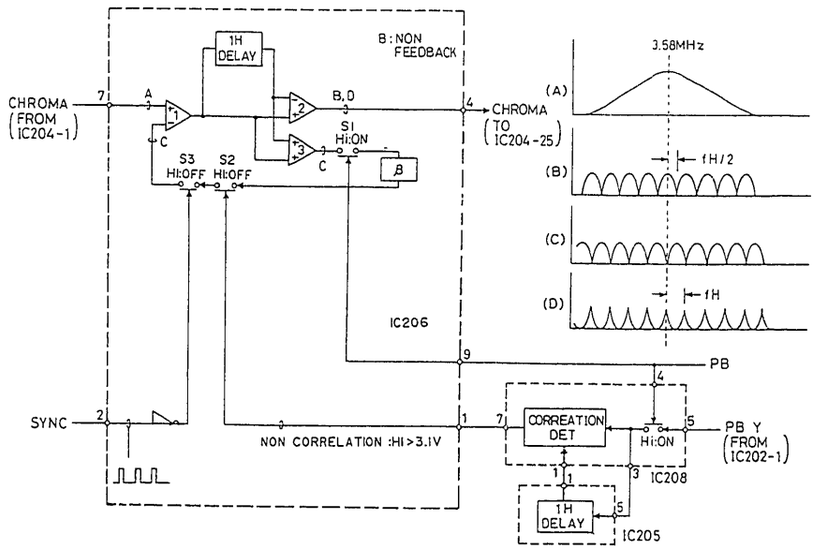


Fig. 4-10 Feedback Comb Filter

In the feedback loop, S3 cuts off feedback during the sync period under the control of the SYNC signal supplied to pin 2.

If the signals occurring 2H and 3H earlier are used, colors diffuse where there is no vertical correlation. To prevent this, S2 cuts off feedback when a lack of correlation is detected. Actually vertical correlation of the playback luminance signal is detected (IC208 performs this) as it is difficult to detect it from the chroma signal because of problems including accuracy of phase.

The playback luminance signal applied to IC208 pin 5 is divided into two; part goes directly to the correlation detector and the other part is output from pin 3 and the 1H-delayed line (CCD: IC205) before entering the correlation detector. This detects any change in the 1H-delayed signal from the two components and, when the difference of amplitude exceeds a certain level, judges that correlation does not exist and sets pin 7 to "Hi". (Hi: more than 3.1V)

This comb filter is also used to separate the chroma signal from the composite video signal during recording by this VTR. However, since pin 9 goes "Lo" during recording, there is no feedback.

4-5 VHS HQ System

This VTR is a S-VHS VTR with upward compatibility with ordinary VHS VTRs, that is, VHS recording and playback are possible.

For recording/playback using VHS, the VHS HQ system for high picture quality in the VHS system is provided. The VHS HQ system used in this VTR consists of the following.

4-5-1 Higher white clipper

When the high-frequency components are boosted by the preemphasis circuit, overshhots occur in the signal waveform, and when the signal is frequency modulated, overmodulation occurs at the higher section of the white peak level, causing the picture quality to deteriorate (by black/white inversion). To prevent this a white clip circuit is provided at the input of the FM modulator.

Since the characteristics of the VTR and video tape have been greatly been improved, black-and-white inversion hardly ever occurs, and so if the clip level is raised by 20%, the pulse response characteristics can be improved. As a result, the rise (edges) of the waveform where black changes to white in the TV picture can be reproduced more clearly.

4-5-2 Detail enhancer

This raises the 3 - 4-MHz low-level high-frequencies according to the input level of video signal. As the detail enhancer does not work during playback, the overall high-frequency characteristics are emphasized and the details, for example, grasses, hair, etc. can be reproduced clearly.

4-5-3 Luminance noise reduction circuit

The luminance noise reduction uses a 1H delay circuit to form a line correlative feedback noise canceller. This feeds back the video signal 1H delayed in the base band to reduce non-correlative noise.

4-6 Video I/O Circuits (Fig. 4-11)

This section selects the inputs and outputs of the video recording/playback circuits and digital circuits. The following ICs switch the signals.

4-6-1 Selection of input signal to the recording circuit

(1) Selection of line/tuner: IC301

IC301 selects either of the line and tuner inputs and supplies it to IC303 and IC305, according to the LINE signal from the system control microprocessor (μP).

(2) Recording in digital mode: IC305

IC303 permits the recording of pictures in digital mode.
In the ordinary record mode, the line/tuner signal comes from IC301 to IC1252. In the digital record mode, the output of the digital circuit is selected. This selection is controlled by the DIGITAL REC signal supplied from the digital circuit. Q310 provided at the output of IC305 turns off during play to prevent the playback signal from leaking to the EE circuit.

(3) Switching signal path of composite/separate input: IC1252

- IC1252 (S5) -
This selects either the composite video signal coming from the line/tuner or the luminance signal coming from the separate Y/C input and supplies it to the luminance recording circuit and IC1202 (S1), according to the Y/C CONT.2 signal from IC1251.

- IC1202 (S1) -
This selects either the chroma signal coming from the separate Y/C input or the composite video signal from IC1252 (S5) and supplies it to the chroma signal recording circuit, under the control of the Y/C CONT.1 signal.

4-6-2 Processing of digital circuit I/O signals

The input and output of each section other than from the line/tuner are separate chroma and luminance signals, but the input and output of the digital circuit are composite video signals.

So, a Y/C mixer (included in IC1251) is provided for the video playback circuit and separate Y/C input and it converts separate chroma and luminance signals into a composite video signal and supplies it to the digital circuit.

The dual comb filter (IC1253) provided at the output of the digital circuit converts the composite video signal into separate signals and supplies them to the separate Y/C output.

4-6-3 Selection of signal input to the digital circuit

(1) Switching signal path depending on record/play mode: IC303
The EE input signal (IC303 pin 4) of the digital circuit is the line/tuner signal from IC301 during playback and only the line input signal during recording. The output goes to IC1252 (S3).

During recording, the tuner signal is sent through a separate lines of the EE circuit in IC201 and the OSD circuit.

(2) Selection of EE input signal: IC1252 (S3)

S3 selects either the line/tuner video signal coming from IC303 or the video signal that comes from the separate Y/C input and has its luminance and chroma components mixed in IC1251, according to the Y/C CONT.2 signal supplied from IC1251. The selected signal is supplied to the digital circuit.

(3) Selection of PB input signal: IC1252 (S1)

S1 selects either the video signal that comes from the playback circuits and has its luminance and chroma components mixed in IC1251 or the EE tuner signal that comes from the OSD circuit, according to the Y/C CONT.3 signal supplied from IC1251. The selected signal is supplied to the digital circuit.

4-6-4 Selection of output signal to separate Y/C output

(1) Selection of luminance signal: IC1251 (S1)

S1 selects either the luminance signal supplied from the luminance signal playback circuit or that supplied from the digital circuit and separated from the composite video signal by the dual comb filter, according to a signal supplied from the logic circuit in IC1251.

(2) Selection of chroma signal IC1251 (S2)

S1 selects either the chroma signal supplied from the chroma signal playback circuit or that supplied from the digital circuit and separated from composite video signal by the dual comb filter, according to a signal supplied from the logic circuit in IC1251.

S3 is placed in front of S2 to pass the input signal directly to the output since the chroma recording/playback circuits do not include an EE signal route.
The amp in the next stage of S3 shuts off the chroma signal while the OSD signal is mixed to prevent the OSD signal from being colored.

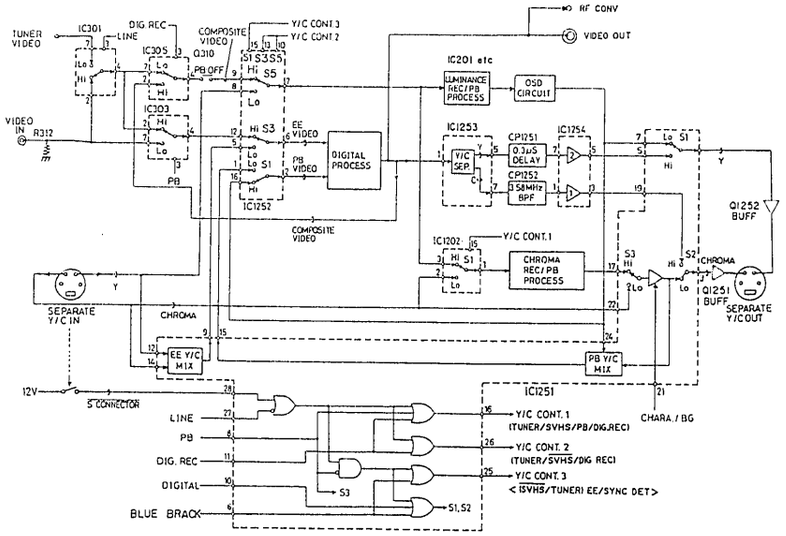


Fig. 4-11 Video I/O Circuit

4-7 Luminance Signal Recording Circuits

The luminacne signal recording circuits consist of the following ICs. The operating mode of each IC is controlled by the PB5V signal and the recording mode is entered when it is "Lo".

4-7-1 Circuit Configuration (Fig. 4-12a)

IC201: S-VHS/VHS AGC
VHS luminance signal record processing
- o 3-MHz LPF
- o Sync clamp, sync separator
- o Preemphasis, dark/white clip, FM modulator, 1.4-MHz LPF

S-VHS/VHS EE signal processing
- o EE amplifier, clip

IC202: Mainly includes playback circuits. The recording signal simply passes through.

IC203: VHS HQ detail enhancer
The signal simply passes through in the S-VHS mode.

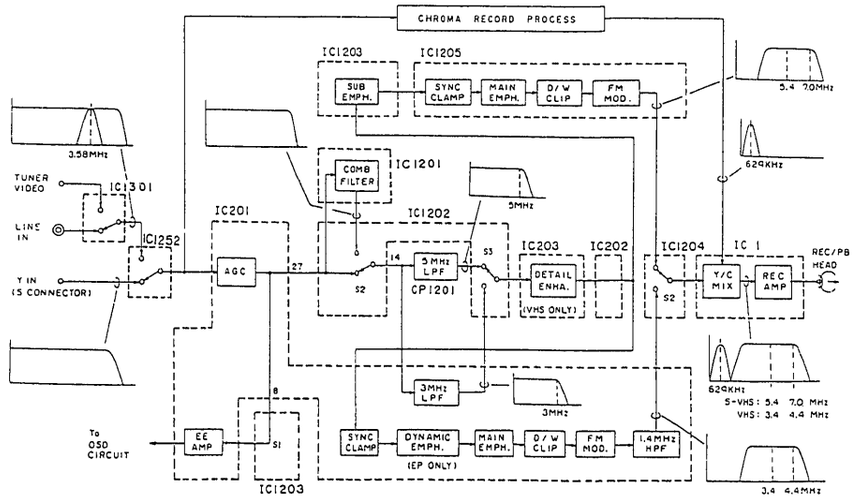
IC1201: Dual comb filter
Separates the luminance signal from the composite video input.

IC1202:
- o Composite/separate input selector (S2)
- o S-VHS/VHS recording band selector (S3)

IC1203: S-VHS subemphasis

IC1204:
- o S-VHS/VHS mode discriminator
- o S-VHS/VHS recording signal selector (S2)
- o Sync signal selector (S4/S5)

IC1205: S-VHS luminance signal record processing
- o Sync clamp, sync separator
- o Preemphasis, dark/white clip, FM modulator



IC12×× : In S-VHS PCB
IC2×× : In YTJ PCB

Fig. 4-12a Simplified Luminance Record Process Diagram

4-7-2 Operation of Circuits (Fig. 4-12b)

(1) AGC and luminance signal extraction

The recording video signal or luminance signal is suppleid to IC201 pin 1. As the input level may vary, the AGC circuit keeps the video signal level fixed.

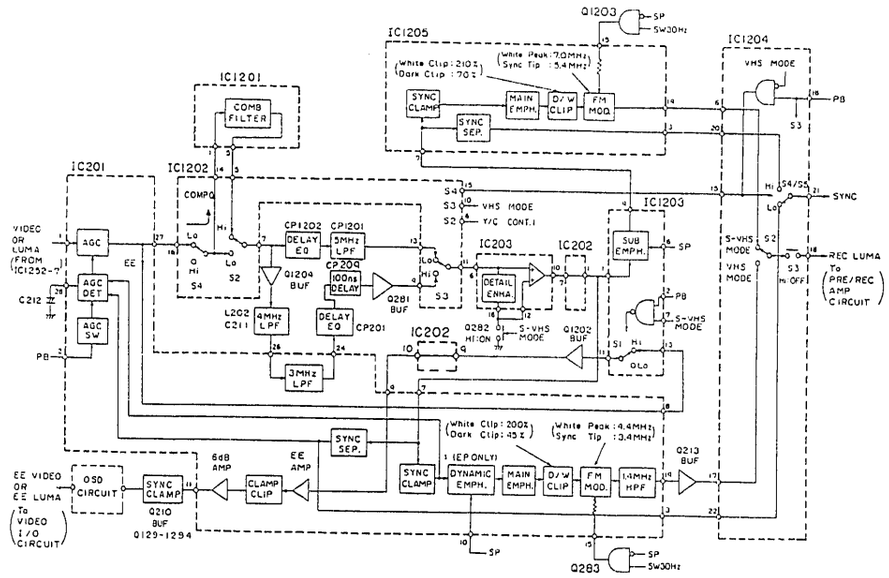
- AGC circuit (Fig. 4-13) -
This consists of the AGC amplifier, clamp and AGC detector. The signal is supplied from the clamp to the AGC detector which detects the level of the luminance signal. The AGC circuit uses the detector output to control the gain of the AGC amplifier and fixes the output level even when the input level varies.

The output of the AGC circuit is supplied to:
- o Recording circuit via pin 27, and
- o EE circuit via pin 8.

The recording signal follows the path described below.

Since the signal supplied from the separate Y/C input is a separated luminance signal, it can be supplied to the recording circuit without being modified. However, the signal from the line input/tuner is a composite video signal, it must be separated to extract the luminance signal.

After passing through the AGC circuit, the recording signal, if it is a luminance signal, is supplied directly to IC1202 (S4) and, if it is a composite video signal, it enters the dual comb filter and the separated luminacne signal is supplied to IC1202 (S2).



IC12×× : In S-VHS board
IC2×× : In YTJ board

Fig. 4-12b Luminance Record Processing Circuit

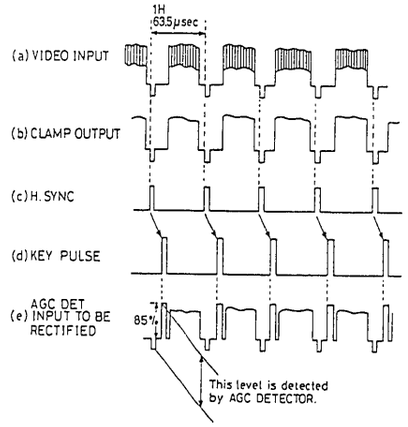


Fig. 4-13 AGC Detector Waveform

S2 switches the signal path according to the Y/C CONT.1 signal supplied from IC1251. The output of S2 passes along separate paths depending on the S-VHS/VHS mode and, after passing through the LPFs that determine the recording bandwidth, it returns to IC1202.

S-VHS path:
The signal goes through the delay equalizer (CP1202) and 5-MHz LPF (CP1201) to pin 13 and further to S3.

VHS path:
The signal goes through the 4-MHz LPF (L202 and C211), 3-MHz LPF (IC201), delay equalizer (CP201) and 100 nsec Delay (CP209) to pin 9 and further to S3.

The delay equalizers compensate for the delay characteristics of the LPFs and deviation of timing with respect to the chroma signal.

The 100 nsec. delay circuit (CP209) delays the signal in the VHS path by 100 nsec. to match the delay times of the signals passing through the VHS and S-VHS pathes.

S3 switches the signal path according to the VHS MODE signal supplied from IC1204. The output of S3 is supplied to the detail enhancer (IC203).

(2) Detail enhancer (Figs. 4-14 and 4-15)

Being included in VHS HQ technology, this operates only in VHS mode. In the S-VHS mode, the output (pin 16) of the detail enhancer is grounded by Q282 and the input signal goes directly to the output.

The detail enhancer enhances the level at around 3-4 MHz according to the video input level. As the detail enhancer does not work during playback, the overall high-frequency characteristics are emphasized and the details, for example, grasses, hair, etc. can be reproduced clearly.

The output goes through IC202 pins 7 and 1 to the subemphasis circuit (IC1203) in the S-VHS mode or to the clamp (IC201) in the VHS mode.

(3) Subempahsis (IC1203)

This is provided exclusively for S-VHS and works together with the main emphasis circuit that comes later to improve the S/N. The amount of emphasis is fixed in

main emphasis but subemphasis is nonlinear, that is, the amount of emphasis varies with the input level.

Subemphasis is to raise the level of high-frequency components, if their level is low, during recording as they are very susceptible to noises. The emphasized level will be deemphasized to restore teh original level during playback. The emphasis parameter will be changed depending on whether operation is in SP and EP according to the SP signal applied to pin 6.

The output is supplied to the sync clamp in IC1205.

(4) Sync separator and clamp
- Clamp -
This fixes the sync tip (DC level) independently of the variation in the video level. The output is supplied to the emphasis circuit.

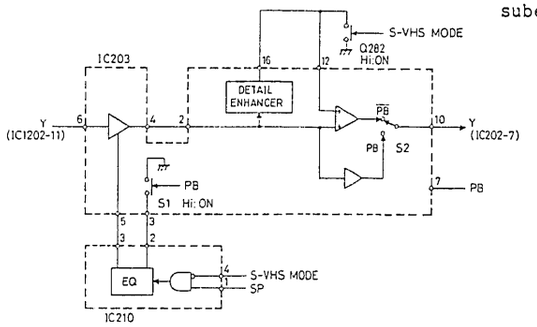


Fig. 4-14 Detail Enhancer & PB Equalizer

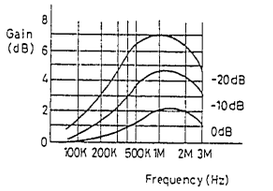
- Sync separator -
This separates the sync signal from the luminacne signal. The output is supplied to the sync signal selector (IC1204-S4/S5) via pin 3.

- Sync signal selector (IC1204-S4/S5) -
This selects the sync signal separated by the sync separator in IC201 normally, but selects the sync signal separated by the sync separator in IC1205 only in the S-VHS play mode.

The sync signal comes to:
- o IC204 (chroma signal processing), and
- o the servo circuit that controls the cylinder motor during recording.

(5) Preemphasis, dark/white clip and FM modulator
- Preemphasis (Fig. 4-16) -
The levels of high-frequency components are emphasized during recording as they are susceptible to noise.

S-VHS path:
Main emphasis (fixed emphasis) only as subemphasis is included in IC1203.



Dynamic Preemphasis (VHS-EP)

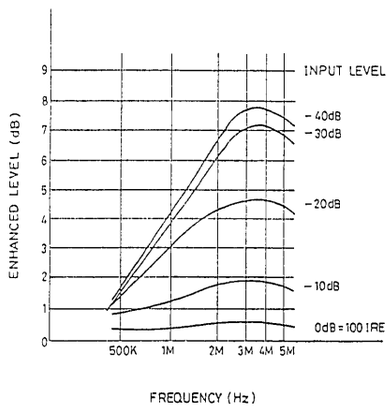


Fig. 4-15 Detail Enhancer Characteristics

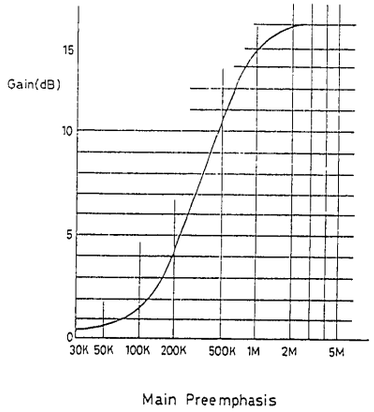


Fig. 4-16 Emphasis

VHS path:
Dynamic emphasis + main emphasis.
Dynamic emphasis is to increase the amount of emphasis when the input level is low. It is active only in the EP mode.

- Dark/white clip -

The preemphasized luminance signal overshoots and undershoots at the leading and trailing edges. If these were to enter the FM modulator, black and white would be inverted due to overmodulation. To prevent this, the signal level is clipped at a certain level.

S-VHS path: white clip 210%, dark clip 70%
VHS path: white clip 200%, dark clip 45%

- FM modulator -

This frequency-modulates the luminance signal and performs carrier-interleaving.

S-VHS path: sync tip 5.4 MHz, white peak 7.0 MHz
VHS path: sync tip 3.4 MHz, white peak 4.4 MHz

(FM carrier-interleaving)
In the EP mode, the FM carrier frequency is 1/2fH-offset by the SW30Hz signal input through pin 16 for every field (the CH-1 carrier is made higher by 1/2fH) to prevent beat interference caused by the adjacent tracks during playback.

In the VHS path, a 1.4-MHz HPF follows the FM modulator.

The lower sideband of the frequency-modulated luminacne signal would extend to low frequencies and interfere with the down-converted chroma signal (629 ±500 kHz). Components under about 1.4 MHz are removed to eliminate this problem.

The S-VHS path does not need any HPF as the FM luminance signal is at high frequencies.

The FM luminance signal goes from pin 19 to IC1204.

(6) Switching over S-VHS and VHS recording signals
S2 in IC1204 performs this switching. Controlled by the S-VHS/VHS mode discriminator included in IC1204, S2 selects either the S-VHS recording luminance signal from IC1205 or the VHS recording luminacne signal from IC201. The output is supplied to the recording amplifier.

S3 provided at the output stage of S2 turns off during play to prevent the playback signal from leaking to the recording amplifier circuit.

4-8 Preamplifiers/Recording Amplifiers (for 3-head system) (Fig. 4-17)

The preamplifiers and recording amplifiers are included in IC1P.

4-8-1 Recording operation

The recording luminance signal comes from IC1204 and goes to the Y/C mixer past the recording equalizer and AGC circuit. The Y/C mixer mixes the luminance signal with the recording chroma signal from IC209. The recording equalizer enhances the level at 1-3 MHz to flatten frequency response of the signal to be recorded. The level is set about 3 dB higher in the VHS mode than in the S-VHS mode.

The recording current passes S9 and comes to the recording amplifeir and the heads. S5 terminates the CH-1 head during recording and S7, the CH-2 head. The voltage drop occurring in the terminating resistor connected to S7 is fed back to the AGC circuit and AGC is applied to the recording current.

4-8-2 Playback operation

S4 turns on and the head outputs enter IC2P.

S2 selects the CH-1 preamplifier output when SW30Hz is "Lo" and the CH-2 preamplifier output when SW30Hz is "Hi".

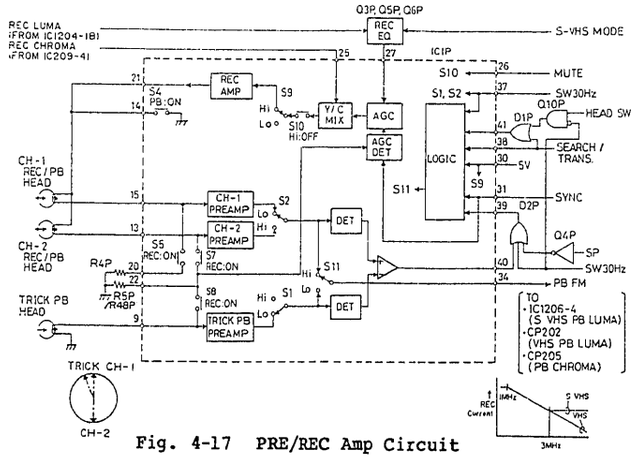


Fig. 4-17 PRE/REC Amp Circuit

S11 selects the output of the recording/playback head and the selected signal comes to the video circuits via pin 34. S11 is controlled by the S11 control signal from the logic circuit (LOGIC).

4-8-3 Trick play operation
During SP search, the output of the trickplay head that is installed adjacent to the CH-1 head the output of which is higher is selected. This allows a section that appeared as noise in the picture previously to be replaced by the output of the trickplay head only for CH-1.

Logic circuit control signals
Pin 41: FH SWITCH
Pin 38: SEARCH/TRANSIENT
These two signals are matrixed to select three heads.

Pin	Pin	Selected heads	Mode
Lo	Lo	CH-1/CH-2	Normal play
Lo	Hi	TRICK/CH-2	Still
Hi	Hi	CH-1 or TRICK/CH-2	SP search

Pin 40: COMPARATOR OUT
This is an comparison output between the recording/playback head and the trickplay head. "Hi" when the recording/playback head output is higher. Used to select the head producing a higher output in the SP search mode.

Pin 39: COMPARATOR IN
When pin 38 is "Hi", this input is applied to S11. Pin 31 is an input to select the head from which the FM output is higher in the SP search mode.
The $\overline{SP}$ and SW30Hz signals are also input to pin 39 through the OR circuit (D2P).

The $\overline{SP}$ signal goes "Hi" in the EP mode and S11 selects the recording/playback head. The SW30Hz signal goes "Hi" during the CH-2 period. Therefore, when these two signals are input, that is in the CH-2 period during SP search, during EP search, the outputs are not compared.

Pin 31: SYNC
Composite sync signal input. This times selection to produce a higher output with the horizontal sync signal.

Pin 37: SW30Hz
Basic head switching signal.

4-9 Luminance Signal Playback Circuits

The luminance signal playback circuits consist of the following ICs. The operating mode of each IC is controlled by the PB5V signal, namely, the playback mode is entered when it is "Hi".

4-9-1 Circuit Configuration (Fig. 4-18a)

IC201: VHS luminance signal playback processing
- o Playback AGC, dropout detector
- o Limiter, FM demodulator, deemphasis
- o 3MHz LPF
- o Noise canceller, squelch, sync separator

IC202: o Luminance noise reduction/ dropout compensator

IC203/IC210: These compose an equalizer.

IC205: 1H-delay line. The 1H-delayed signal is supplied to the luminance noise reduction circuit and dropout compensator.

IC1201: Dual comb filter
This attenuates the chroma component in the luminance signal during playback.

IC1202: o S-VHS/VHS playback signal selector (S4)
- o S-VHS/VHS playback band selector (S3)

IC1203: o S-VHS subemphasos
- o S-VHS/VHS playback signal selector (S1)

IC1204: o S-VHS/VHS mode discriminator

IC1205: S-VHS luminance signal playback processing
- o Playback AGC, dropout detector
- o Limiter, FM demodulator, deemphasis
- o Noise canceller, sync separator

IC1206: S-VHS 5-MHz peaking

4-9-2 Operation of Circuits (Fig. 4-18b)

(1) Playback equalizer and chroma trap
The playback equalizer compensates for the heads' playback frequency response as the preamplifeir in IC1P has a flat frequency response. The playback equalizer consists of a peaking circuit that raises the level of components close to the upper limit of the FM carrier frequency.

The chroma trap removes the 629-kHz chroma signal.

S-VHS path:
IC1206 (5-MHz peaking), CP1203 (8.3-MHz peaking), L1215 and C1245 (chroma trap)

VHS path:
CP202 (4.6-MHz peaking), L203 and C213 (chroma trap)

The peak shift circuit consisting of the components, R210, C215, Q206 and Q207 which are connected to CP202, operates during the SP trick play mode. It lowers the peaking frequency to cancel white noise appearing in noise bands during trick play (mainly in search) so that vertical jitter and skew occurring when the vertical sync signal is affected by white noise should not occur.

(2) AGC and dropout (DO) detector
The playback signal, from the playback equalizer, goes through pin 20 to the AGC circuit in IC1205 in the S-VHS mode and to that in IC201 in the VHS mode. The AGC circuit compensates for differences in the outputs of the heads of different channels and deviation of the outputs. The output of the AGC circuit is applied to the dropout compensator.

The dropout detector detects dropouts of the FM signal occurring due to scratches on the tape. It consists of a limiter, rectifier and LPF. The LPF removes AC components from the AGC output that has passed the limiter. A drop of level originating from a dropout then appears as a change of DC level which becomes the switching pulse that triggers the operation to replace the original signal with the 1H-delayed signal for dropout compensation. The trigger pulse comes from pin 16 to the switching circuit that is part of the luminance noise reduction circuit (1H correlation noise canceller) in IC202. It is the switching circuit that replaces the original signal with the 1H-delayed signal from the CCD 1H-delay line (IC205) when dropout occurs.

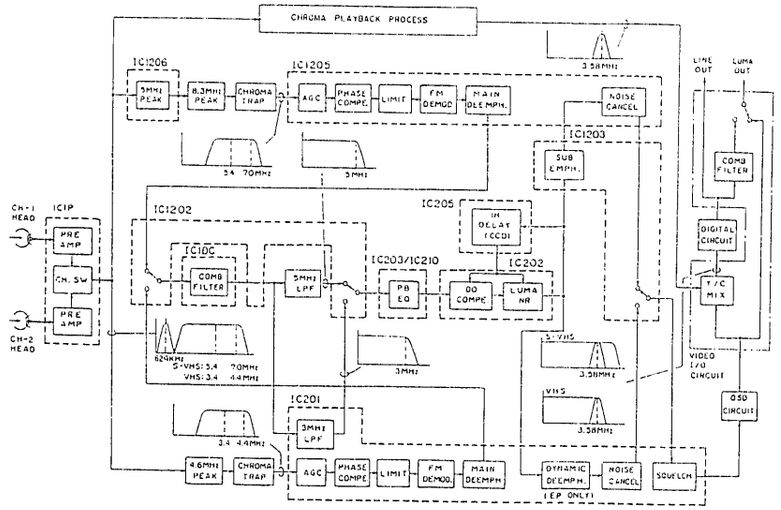


Fig. 4-18a Simplified Luminance Playback Process Diagram

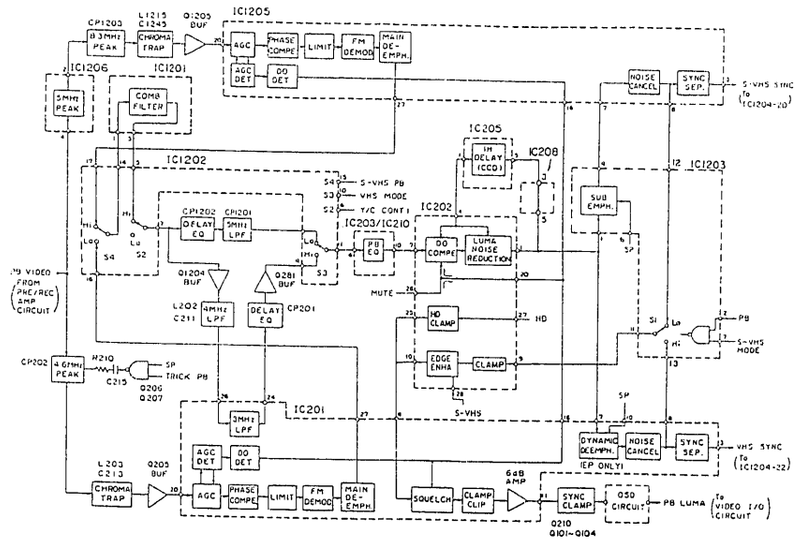


Fig. 4-18b Luminance Playback Processing Circuit

(3) Playback phase compensator, limiter, FM demodulator, chroma bandwidth attenuation

The FM AGC output is supplied to the phase compensator. The equalized playback signal is subject to phase distortion which would cause the demodulated waveform to be distorted. To prevent this, the phase compensator corrects phase distortion caused by the playback equalizer. The output of the phase compensator is supplied to a limiter that removes the lower sideband to play back a normal FM signal. If the recording wavelength is reduced and more preemphasis is applied in order to achieve high-density recording, the FM carrier would become smaller than the lower sideband and, if such a signal were to be demodulated, black and white would be inverted. The limiter prevents this.

AM components are removed from the limiter output by a differential amplifier having a gain of about 40 dB. The output is supplied to the following FM demodulator and demodulated into a luminance signal.

The demodulated signal goes through the main deemphasis circuit to pin 27. The main deemphasis circuit is the reverse of the main preemphasis circuit. The

demodulated signal coming out of pin 27 follows the same path as in recording and the chroma band (at around 3.58 MHz) and spurious bands (S-VHS: over 5 MHz, VHS: over 3 MHz) are attenuated.

S-VHS path:
IC1202 (S4), IC1201 (dual comb filter), CP1202 (delay equalizer), CP1201 (5-MHz LPF).

VHS path:
IC1202 (S4), IC1201 (dual comb filter), L202 and C211 (4-MHz LPF), IC201 (3-MHz LPF), CP201 (delay equalizer).

S3 in IC1202 switches over these signal paths.

The output of S3 goes through the equalizer (IC203/IC210) to the luminance noise reduction circuit/dropout compensator in IC202.

The equalizer consisting of IC203 and IC210 raises the signal near 4 MHz in the VHS SP mode and the signal near 6 MHz in other modes to perform playbck equalization.

(4) Luminance noise reduction circuit/dropout compensator (Fig. 4-19)

IC202 forms the luminance noise reduction circuit. In IC202, the signal applied to pin 7 is added to the 1H-delayed signal coming to pin 4 and the output is supplied to pin 1 with noise cancelled out. Part of the luminance noise reduction is used as the dropout compensator. If the AGC circuit detects a dropout, IC202 receives information through pin 20 and switches S1 to the pin 4 side so that the 1H-delayed signal is substituted for the original signal to compensate for the dropout. The output is applied to the subemphasis circuit of IC1203 in the S-VHS path and to the dynamic deemphasis circuit of IC201 in the VHS mode.

The luminance noise reduction circuit reduces random noise included in the playback signal to improve the S/N by some 2 dB and effectively eliminate noise which would otherwise appear over the screen.

As the original video signal includes almost the same information as adjacent signals, the luminance noise reduction circuit extracts random noise (A) from the original and 1H-delayed signals and adds them with opposite phase to the original signal in order to reduce noise.

The original signal becomes the video signal after being demodulated by IC1205 or IC201. This signal, still involving noise, is supplied to IC202 through pin 7. The 1H-delayed signal produced from the original signal by the CCD 1H-delay circuit (IC205) is supplied to pin 4. From the input to pin 7, a subtractor extracts a noise component as the difference signal. This is applied to the following subtractor with opposite phase. S2, controlled by the DC level applied to pin 5, opens in the trick play mode. The positive input of the subtractor is the original or 1H-delayed signal from S1. S1 that normally selects the original signal switches over to the 1H-delayed signal according to the input to pin 20 when dropout is detected. The input from S7 is subtracted from the input from S1 and, as a result, the video signal having reduced noise comes out to pin 1 of IC202.

(5) 1H-delay circuit (Fig. 4-20)

The CCD 1H-delay circuit drives a CCD counter, timed by a reference clock signal (2 x fsc). On receiving a certain number of clock pulses, it delays the video signal by 1H.

The clock signal is generated as described below.

The signal of 3.58 MHz (fsc) applied to pin 14 is doubled to 2fsc and the filter connected to pin 11 extracts only the 2fsc component as the clock signal.

The clock signal (2fsc) has a period of approximately 0.14 µsec and the input to IC205 pin 5 is delayed by 1H for every 452-bit time (equal to 1H) and the output is supplied to pin 3. From the output, the 3.0-MHz LPF (CP207) removes high-frequency components except the luminance signal and supplies them to the luminacne noise reduction circuit through a buffer.

(6) Subemphasis, dynamic deemphasis and noise canceller

The luminance signal coming from the luminance noise reduction circuit goes to the squelch circuit in IC201 past the following.

S-VHS path:
IC1203 (subemphasis), IC1205 (noise canceller), IC1203 (S1)

VHS path:
IC201 (dynamic deemphasis/noise canceller), IC1203 (S1)

S1 in IC1203 switches over the signal paths.

The sub or dynamic deemphasis circuit restores the original level of the signal emphasized during recording. The deemphasized signal comes to the nosie canceller, in which a limiter removes unclipped, small-amplitude, high-frequency components (mostly noise). The limiter also clips large-amplitude, high-frequency components (corresponding to the edges of a picture). As a result, only noise is removed while the clarity of the picture is not affected. The output of the noise canceller is divided into two; one comes to the sync separator and the other to the squelch circuit in IC201 through IC1203 (S1).

o The sync separator extracts the composite sync signal from the luminance signal and applies it to the chroma and servo circuits.

The HD clamp (video blank) circuit in front of the squelch circuit sets the front porch level of the artificial V. sync pulse slightly higher than the pedestal level to prevent vertical jitter and skew caused by noise that enters the front porch of the artificial V. sync pulse; it also inserts a H. Sync pulse.

(7) Squelch circuit

The squelch circuit cuts off the passage of the video signal when "Hi" is applied to pin 16. The MONITOR CUT signal or the output of the artificial V sync circuit is connected to pin 16. The MONITOR CUT signal supplied from the system control microprocessor rises to "Hi" during loading to inhibit playback output. The output of IC601 (V. DRIVE PULSE circuit) is used for both artificial V sync pulse and recording mute signal to become active during recording pause with the camera and to suppress jitter with the artificial V sync pulse during trick play.

The output of the squelch circuit goes through the clipping circuit and output amplifier (6-dB gain) to pin 11 as the playback video signal.

The clipping circuit clips the video waveform at 125% of the white peak in reference to the sync tip to reduce buzz.

Luminance signal - search, still mode -

During search and still play, the artificial V sync pulse (CH-2: 10H wide at 214 µsec from rising edge, CH-1: position adjustable with variable resistor of the servo circuit) supplied from the servo circuit is transferred to the squelch circuit through the muting control line to stabilize the picture.

4-10 Chroma Signal Recording Circuits

The chroma signal recording circuits consist of the following ICs. Selection of the record/play mode is controlled by the PB5V signal, that is, the record mode is entered when it is "Lo".

4-10-1 Circuit Configuration (Fig. 4-21a)

IC204: Chroma signal record processing
- o ACC, main converter, burst emphasis, color killer, 1.3-MHz LPF
- o 4-phase shifter
- o 4.21-MHz sub converter
- o 3.58-MHz generator, 40fH generator

IC206: Comb filter
Separates the chroma signal from the composite video input.

IC209: 3.58-MHz, 7.16-MHz and 1.4-MHz traps

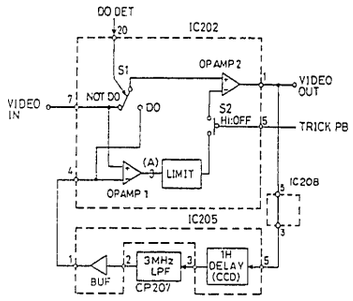


Fig. 4-19 Luminance Noise Reduction and Dropout Compensation Circuit

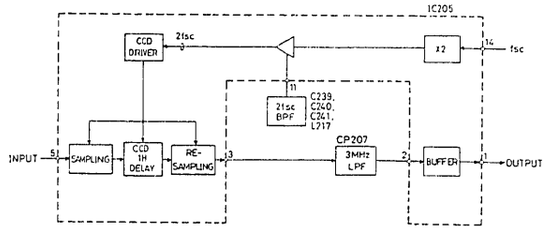


Fig. 4-20 CCD 1H Delay Circuit

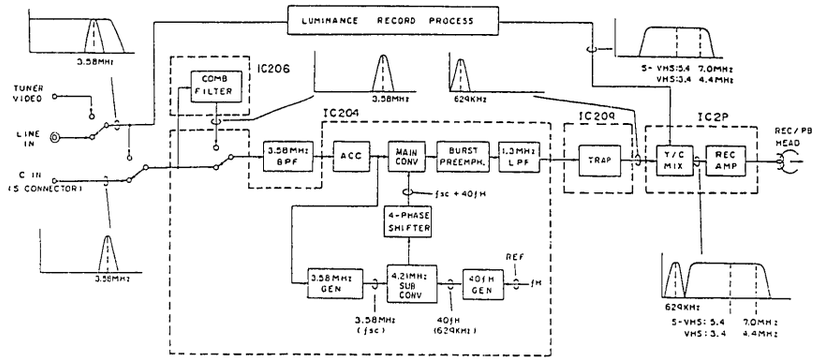


Fig. 4-21a Simplified Chrominance Record Process Diagram

4-10-2 Operation of Circuits
(Fig. 4-21b)

(1) Chroma signal extracter

Since the signal supplied from the separate Y/C input is a separated chroma signal, it can be supplied to the recording circuit without being modified. However, the signal from the line input/tuner is a composite video signal, it must be separated to extract the chroma signal.

Coming from the video I/O circuit, the recording signal, if it is a chroma signal, is supplied directly to IC204 (S8) and, if it is a composite video signal, it enters the comb filter and the separated chroma signal is supplied to IC204 (S8). S8 switches the signal path according to the Y/C CONT 1 signal supplied from IC1251. The output of S8 is delayed by CP203 by 0.1 µsec to match the timing of the luminance signal path in the VHS mode and is then supplied to the 3.58-MHz BPF (CP204). CP204 (3.58-MHz BPF) extracts the components of 3.58 MHz ±500 kHz and supplies the output to the ACC circuit.

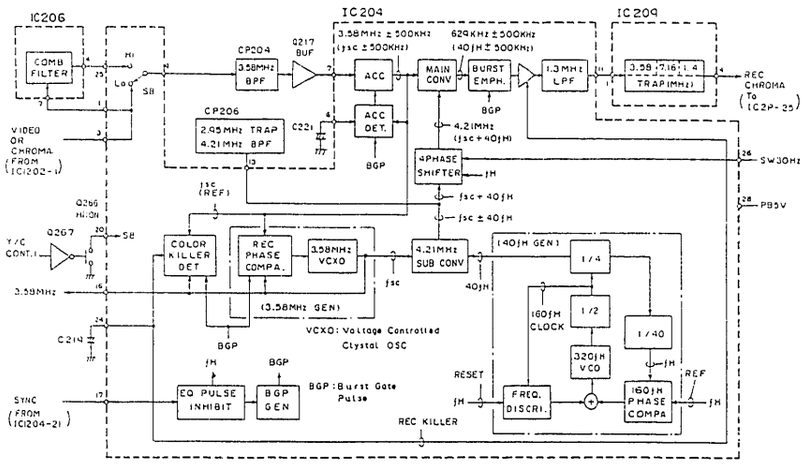


Fig. 4-21b Chrominance Record Process Circuit

(2) ACC (Fig. 4-22)

The ACC amplifier operates just like a keyed AGC. ACC DET (ACC detector) which controls the gain of the ACC amplifier receives the two signals for sync detection.

- o One is the output of the ACC amplifier.
- o The other is the burst gate pulse (BGP). It rises about 3 µsec later than the leading edge of the sync tip of the horizontal sync signal and lasts for 4.8 µsec.

Detecting sync from these signals, the ACC detector extracts the burst signal from the video signal and detects burst level. The output charages C221 connected to pin 6 and, after being fed back to the ACC amplifeir, it fixes the burst level.

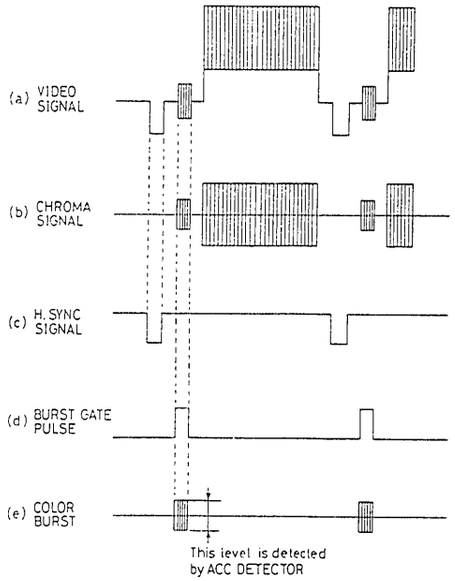


Fig. 4-22 ACC

(3) Main converter

The main converter mixes the chroma signal of 3.58 MHz ±500 kHz with the 4.21-MHz signal of the 4.21-MHz sub converter to down-convert the chroma signal to 629 ±500 kHz.

(4) Burst emphasis

If noise is mixed in the burst signal, the S/N would deteriorate and phase distortion would occur. To prevent this, the burst emphasis circuit raises the burst level by +6 dB.

(5) Color killer

Burst emphasis is followed by the color killer amplifier that cuts off the output according to a control signal supplied from the color killer detector.

When a burst signal is lacking in the recording signal applied to IC204 (i.e. the input video signal is black and white), the color killer cuts off the output to eliminate any chroma component from the recording signal.

(6) 1.3-MHz LPF

This consists of the 1.3-MHz LPF in IC204 and the 3.58, 7.16 and 1.4 MHz traps in IC209.

The 1.3-MHz LPF extracts the difference signal (629 ± 500 kHz) out of the main converter outputs ((4.21 ± 0.5 MHz) ± (3.58 ± 0.5 MHz)).

IC209 in the latter stage removes spurious components which the 1.3-MHz LPF has not removed. The output is supplied to the recording amplifier.

4-11 Chroma Signal Playback Circuits

The chroma signal playback circuits consist of the following ICs. Selection of record/play mode is controlled by the PB5V signal, that is, the play mode is entered when it is "Hi".

4-11-1 Circuit Configuration
(Fig. 4-23a)

IC204: Chroma signal playback processing
- o ACC, main converter, burst emphasis, color killer
- o 4-phase shifter
- o 4.21-MHz sub converter
- o 3.58-MHz generator, 40fH generator

IC206: Feedback comb filter

4-11-2 Operation of Circuits
(Fig. 4-23b)

(1) 1.3-MHz LPF

CP205 (1.3-MHz LPF) extracts the down-converted chroma signal (629 ±500 kHz) from the playback video signal and delivers the output to the ACC circuit in IC204.

The 70-kHz trap (L216, C257) next to the 1,3-MHz LPF (CP205) removes bias frequencies which enter the circuit in the audio dub mode.
The 1.4-MHz trap (L225, C202) removes lower sideband in the luminance signal which was not completely attenuated by the 1.3-MHz LPF.

(2) ACC

Operation is the same as in recording but a signal converted to 3.58 MHz in a latter stage is used to detect the timing, in place of the output of the ACC circuit.

(3) Main converter

The main converter mixes the down-converted chroma signal (629 ±500 kHz) with the 4.21-MHz signal of the 4.21-MHz sub converter to convert the chroma signal to 3.58 MHz ±500 kHz.

(4) 3.58-MHz BPF

The 3.58-MHz BPF extracts the difference signal (3.58 MHz ± 500 kHz) out of the main converter outputs ((4.21 MHz ± 500 kHz) ± (629 ± 500 kHz)).

(5) Burst deemphasis

This reduces the burst level by 6 dB to restore the original level as the burst signal was raised by 6 dB during recording.

(6) Feedback comb filter (Fig. 4-24)

The comb filter consists of a 1H-delay line which removes corsstalk components from the chroma signal.

(7) Color killer

Operation is the same as in recording. The output is supplied to the video I/O circuits.

4-12 40fH Generator/3.58-MHz Generator Circuits

4-12-1 General

The 40fH generator/3.58-MHz generator circuits convert the chroma carrier frequency;

- o from 3.58 MHz to 629 kHz during recording, and
- o from 629 kHz back to 3.58 MHz during playback.

At the same time, they advance the signal phase of each channel by 90° for every 1H in CH-1 and delay it by 90° in CH-2, while being synchronized with the SW30Hz signal and horizontal sync signal.

During playback, they delay the signal phase by 90° for every 1H in CH-1 and advance it by 90° in CH-2, to restore the original phase.

Frequency conversion is done by the main converter. It receives a subcarrier (4.21 MHz) from the 4.21-MHz sub converter explained later. The subcarrier is a composite signal including the following signals:

- o 3.58 MHz processed by the 3.58-MHz generator
- o 629 kHz processed by the 40fH generator

The 3.58-MHz generator has to supply an accurate 3.58-MHz signal in the record and play modes.

The 40fH generator has to supply an accurate 629-kHz signal in the record and play mode.

The 90° phase rotation is performed by the 4-phase shifter circuit.

4-12-2 3.58-MHz generator circuit

The role of the 3.58-MHz generator is to supply an accurate and stable 3.58-MHz signal. It locks the signal to be in phase with the burst signal during recording. During playback, it becomes a 3.58-MHz fixed quartz oscillator.

(1) Record mode (Fig. 4-21b)

A closed loop is formed with 3.58-MHz VCXO and the recording phase comparator. The output frequency of the 3.58-MHz VCXO is locked to the burst signal.
The recording phase comparator receives the following three signals.

- o 3.58-MHz VCXO output
- o Chroma signal from the ACC amplifier
- o Burst gate pulse from the burst gate

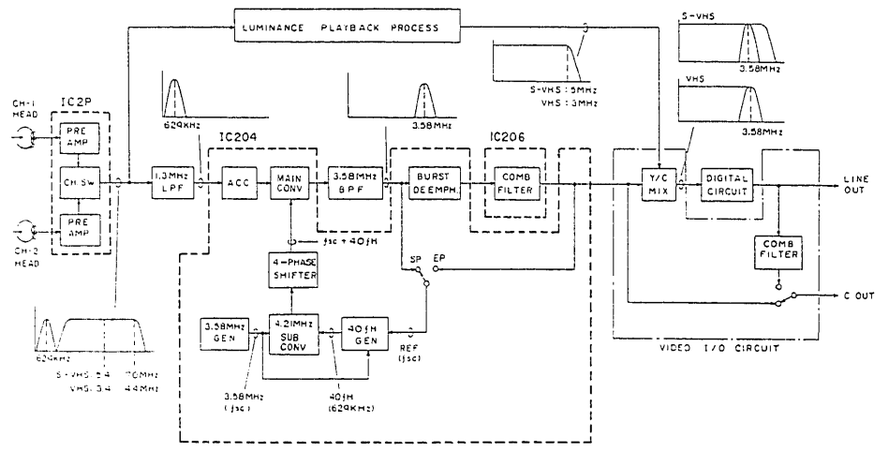


Fig. 4-23a Simplified Chrominance Playback Process Diagram

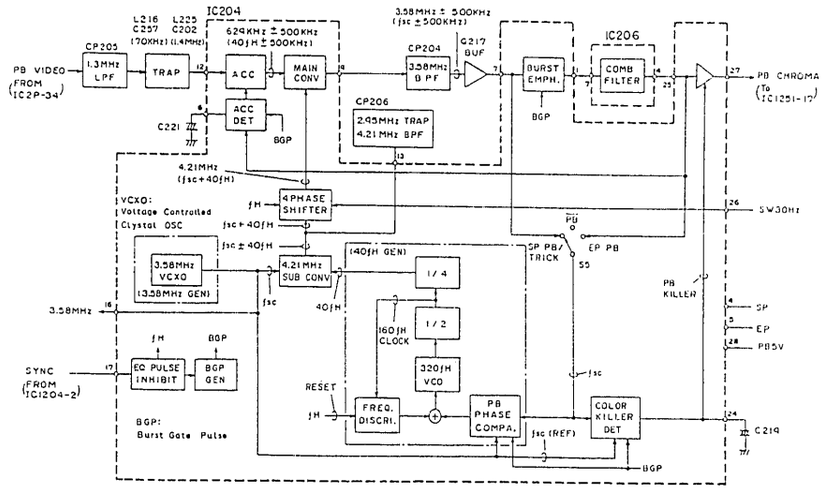


Fig. 4-23b Chrominance Playback Processing Circuit

pulse generator.

The recording phase comparator;

- o Receives these signals,
- o Detects timing,
- o Extracts the burst signal from the video signal, and
- o Compares the phase of the 3.58-MHz VCXO output with that of the burst signal (3.58 MHz).

The output of the recording phase comparator is fed back to the 3.58-MHz VCXO so that its output is locked to be in phase with the burst signal. The 3.58-MHz VCXO output is supplied to the 4.21-MHz sub converter and added to the 629-kHz output of the 40fH generator.

(2) Play mode (Fig. 4-23b)

The recording phase comparator is idle during playback. The closed loop is released and the 3.58-MHz VCO becomes a 3.58-MHz fixed oscillator. The accuracy of the output frequency depends on that of the quartz crystal.

4-12-3 40fH generator circuit

The role of the 40fH generator is to oscillate accurately and stably at 629 kHz (40fH). The 629-kHz (40fH) VCO is locked to be in phase with the horizontal sync signal during recording, the phases of the 3.58-MHz VCXO and burst signal in the chroma signal are compared to control the 320fH VCO output.

(1) Record mode (Fig. 4-21b)

A closed loop is formed with a 320fH VCO and the 160fH phase comparator. The output frequency of the 320fH VCO is locked to the horizontal sync signal.

The 160fH phase comparator receives the following two signals:

- o Division of the 320fH VCO output by the divide-by-320 circuit
- o Horizontal sync signal given from IC204 pin 17 through the EQ pulse inhibit (horizontal sync signal gate)

The 160fH phase comparator compares the phase of the output of the divide-by-320 circuit with the horizontal sync signal (fH) and the output is fed back to the 320fH VCO to lock its output frequency to the horizontal sync signal.

The output of the 320fH VCO passes divide-by-2 and divide-by-4 circuits, that is, it is divided by 8.

The output of the divide-by-4 circuit is 629 kHz (40fH). The output is applied to the 4-phase shifter to control phase rotation.

(2) Play mode (Fig. 4-23b)

During play, the burst signal frequency fluctates due to jitter. To remove these fluctuations, a closed loop of 320fH VCO is formed to compare the phase of the burst signal in the playback chroma signal with that of the 3.58-MHz continuous signal which is free from frequency variations and transmit the frequency variations to 4.21-MHz signal.

The playback phase comparator receives the following three signals:

- o 3.58-MHz oscilaltor output
- o Playback chroma signal from S5
- o Burst gate pulse from the burst gate pulse generator.

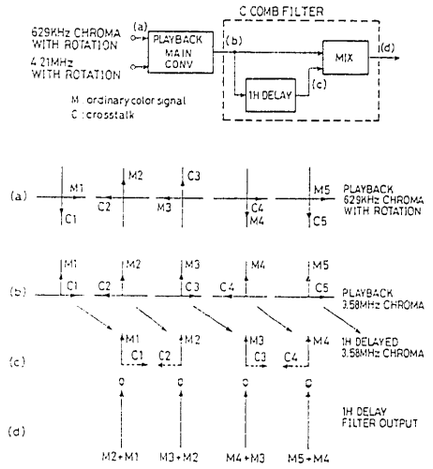


Fig. 4-24 Color Crosstalk Cancellation

The playback phase comparator receives these signals, detects their timing, extracts the burst signal from the playback video signal, and compares the phase of the burst signal with the reference output of a 3.58-MHz oscillator. The resultant signal of comparison is fed back to the 320fH VCO circuit to control the oscillation frequency of the 320fH VCO.

4-12-4 4.21-MHz sub converter

The 4.21-MHz sub converter produces a 4.21-MHz subcarrier that is used by the main converter which frequency-converts the chroma signal. The 4.21-MHz signal is obtained by adding the 40fH signal (629kHz) produced by the 40fH generator and the 3.58-MHz signal (fsc) produced by the 3.58-MHz generator. The fsc±40fH signal thus obtained is applied to the 4.21-MHz BPF/2.95-MHz TRAP (CP206) connected to pin 13 where removes the difference component, fsc±40fH, to create an fsc±40fH signal (4.21-MHz). This signal is applied to the 4-phase shifter.

4-12-5 4-phase shifter
(Figs. 4-25 and 4-26)

The 4-phase shifter generates a 4.21-MHz, 4-phase signal from the 4.21-MHz input signal and applies the output to the main converter.

The phase of the 4.21-MHz signal is shifted by a resistor (R) and a capacitor (C) by about 45°. The signal Er developed across the resistor and the signal Ec across the capacitor have phases that are different by 90°. From Ec and Er, four limiting amplifiers generate four 4.21-MHz signals. These signals have a fixed amplitude but varying phases, 0°, 90°, 180° and 270°. They are applied to V1-V4 respectively.

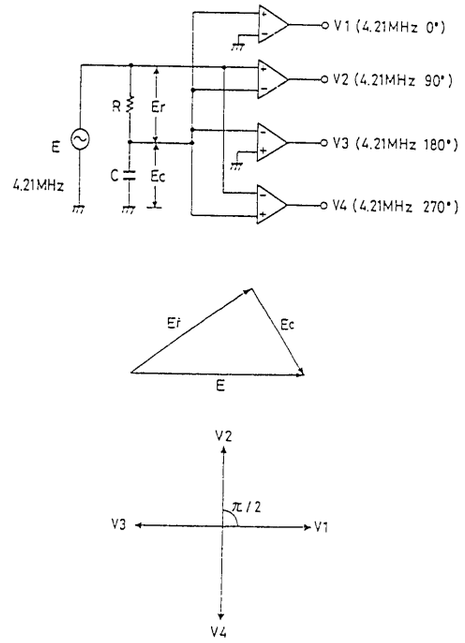


Fig. 4-25 4 Phase Shift Circuit Operation Principle

Gate pulses are obtained by applying the horizontal sync pulse selected by the horizontal sync gate to a ring counter. The phase of the gate pulse varies depending on the level of the SW30Hz signal applied from pin 26.

In the first field of the CH1 video head, the gates conduct in the order 1-2-3-4. As a result, the phase rotates from 0° to 90° to 180° to 270°. In the second field of the CH2 video head, the gates conduct in the order 1-4-3-2. So, the phase rotates from 0° to 270° to 180° to 90°. This is equivalent to the required rotation, from 0° to -90° to -180° to -270°.

When the SW30Hz signal is "Lo", one of the 4.21-MHz signals is selected in every cycle of the fH signal so that the signal phase advances by 90° from one cycle to the next. When the SW30Hz signal is "Hi", selection is done in such a way that the signal phase is delayed by 90° from one cycle to the next.

4-12-6 Color killer detector

The color killer detector detects the burst signal in the video signal to control the output of the chroma signal. It receives the burst gate signal and the chroma signal from the ACC amplifier, detects its timing, and extracts the burst signal, if it is present. When the burst signal is detected, the killer amplifier outputs the chroma signal.

4-12-7 Frequency discriminator

The 320fH VCO receives not only the phase detector output but also the output of a frequency discriminator to remove any playback time axis errors. The output of the 320fH VCO is variable over a wide range. The frequency will deviate from 5.04 MHz during transition times like the switching on of the power supply. At this time, the frequency discriminator operates to bring the frequency of the 320fH VCO correctly to 5.04 MHz. The frequency discriminator continues to work until the frequency is locked at the

right value (320fH). This operates accurately, simulating digital operation. When the 320fH VCO is oscillating right at 320fH, it produces 320 pulses every 1H. If it is oscillating at 324fH, the number of pulses per 1H is 324. So, the oscillation frequency can be determined by counting the number of pulses per 1H.

The 1H interval can be defined very accurately as it is the repetition interval of the horizontal sync signal.

Actually the frequency discriminator detects the frequency with offsets of ±1/2 fH to improve response. The pulses are counted for the 4H period to discriminate the 1/2 fH offsets. A control signal is applied from a decoder so that the output frequency of the 320fH VCO rises when the pulse count during 4H is less than 638 and the frequency falls when the pulse count is more than 642.

4-12-8 Burst gate pulse generator

The horizontal sync signal gate circuit (EQ pulse inhibit) extracts H.SYNC (fH) pulse from the composite sync signal (SYNC) applied to pin 17 by removing equalization pulse. The H.SYNC (fH) pulse triggers a monostable multivibrator in the burst gate pulse generator to generate a burst gate pulse synchronized with the burst signal.

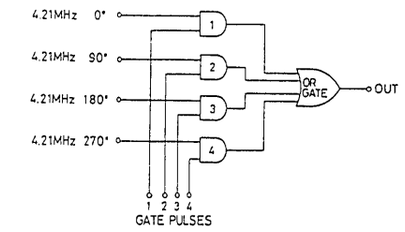


Fig. 4-26a 4-Phase Shifter

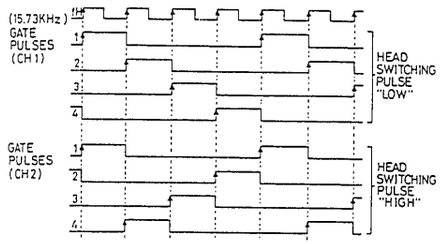


Fig. 4-26b Gate Pulses

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